Application Note

AP603 Push-Pull 470-860 MHz Reference Design

Summary

The AP603 is a high dynamic range power amplifier in a lead-free/RoHS-compliant 5x6mm power DFN SMT package. It features an internal active-bias circuit that provides temperature compensation and dynamic bias adjustment. The input and output matching networks are realized with surface mount components allowing the part to be tuned over a wide range of frequencies. This application note examines the performance of the AP603 in a push-pull configuration tuned for 470-860 MHz. In this frequency range, the amplifier has approx. 14.5dB gain, good gain flatness, +41 dBm P1dB, and 2.5% EVM (802.16-2004 OFDMA, 64QAM-1/2,1024-FFT, 20 symbols, 30 subchannels signal, 9.5 PAR @ 0.01%) at 7dB of back-off from P1dB.

Measured RF Performance Summary

Frequency (MHz)	Units	400	600	800
Small Signal Gain	dB	14.8	14.2	15.1
Input Return Loss	dB	-5.5	-6.8	-11.0
Output Return Loss	dB	-8.5	-10.8	-7.2
IMD3 @ 33 dBm/tone (Δf=1MHz)	dBc	-56	-46	-42
OIP2 @ 37 dBm/tone	dBm	72.5	na	na
EVM @ 7dB back-off	%	2.5	2.5	2.5
Output P1dB	dBm	42.2	40.7	42.8
Quiescent Current, Icq	mA	320		
Vpd, Vbias	V	+5		
Vcc	V	+28		

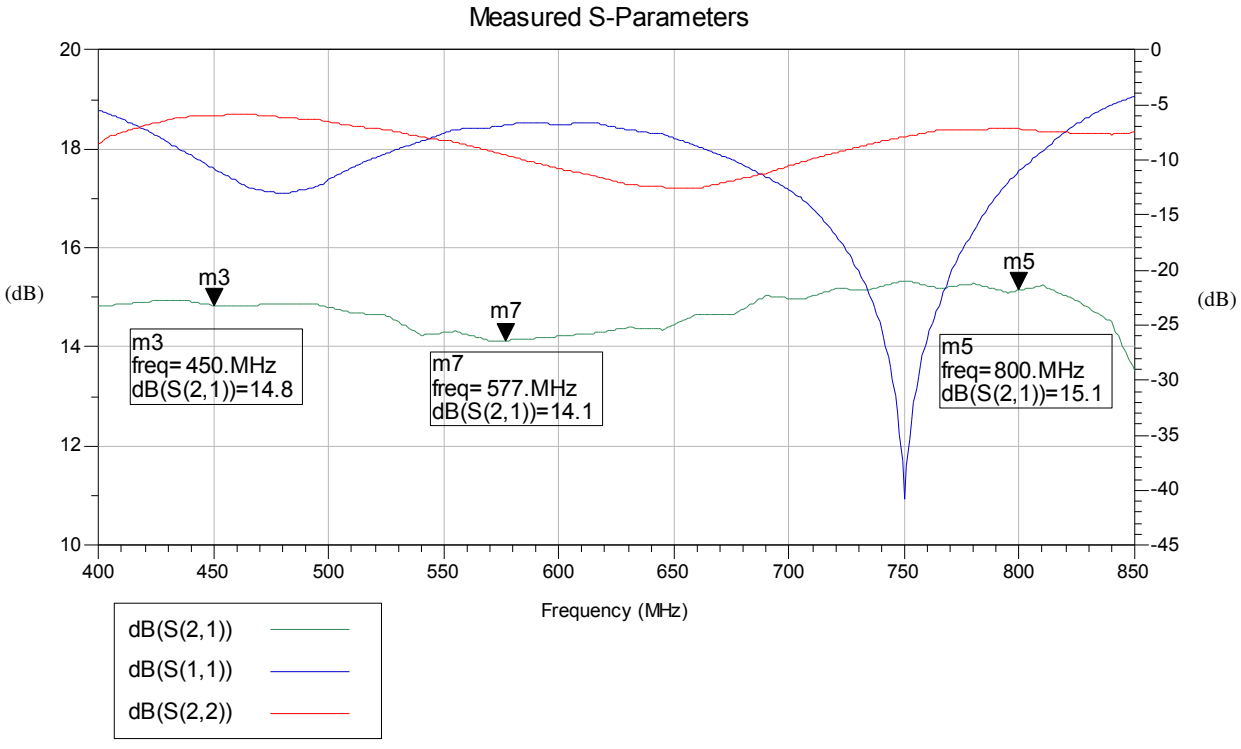


Table of Contents

List of Figures

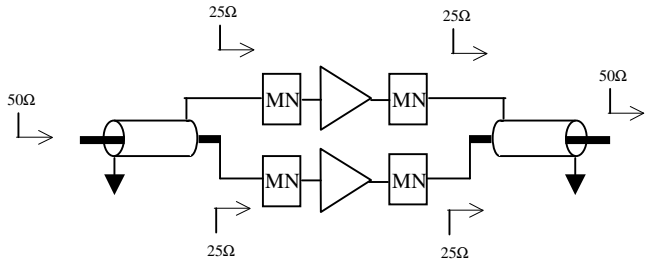
List of Tables

Background

Discussion of the Push-Pull Topology

The push-pull topology consists of two amplifiers operating in parallel with signals 180° out of phase. One implementation (Figure 1) uses a transmission-line balun to convert a single-ended input signal to a differential signal that is applied between the inputs of the two parallel amplifiers. Matching networks (MN) are used at the input and output to present appropriate impedances to the device terminals. At the output of the amplifiers a second balun is used to convert the differential signal back to a single-ended signal.

Figure 1 - Push-Pull Amplifier Block Diagram



At the cost of using two amplifiers (and thus twice the power consumption) and two baluns the following benefits are achieved:

1. 3dB higher P1dB – since the output power of the amplifiers is combined each amplifier operates 3dB lower than the total output power of the push-pull amplifier,
2. Reduction of 2nd order IMDs (higher OIP2) – the 2nd order distortion products of each amplifier are in-phase and therefore cancel because the output signal is taken differentially. Because the 2nd order rejection is dependent on how well the two signal paths are matched, push-pull amplifiers are sometimes implemented with adjacent transistors on a single die to minimize process variation. The AH22S is an example of this.
3. Lower Q impedance transformations resulting in wider bandwidth – the baluns typically have 50Ω unbalanced input impedance and 25Ω balanced input impedance so the input and output matching networks have lower impedance transformations compared to a single-ended amplifier and hence lower Q and wider bandwidth.

Because of the rejection of 2nd order distortion products (IMD2), push-pull amplifiers are often used in broadband applications in which these products fall in-band such as in cable TV and public radio applications.

AP603 Push-Pull Reference Design

Matching Network Design Methodology

Prior to this work an AP603 450MHz to 800MHz reference design had been created[1] using a standard AP60x Rogers Ultralam eval board. The load impedance of this design (as seen by the AP603) was simulated with AWR (Figure 2) and the output matching network was retuned to provide a similar load impedance with Z_o = 25Ω rather than 50Ω (Figure 3). The input match was then tuned (Figure 4) to provide a broadband input match from 400MHz to 800MHz (Figure 5). Note, a large-signal ADS model was not available at this time and s-parameters (available from the website) were used. The small-signal performance was then simulated (Figure 6) in a push-pull configuration.

[1] TQS Application Note – AP603 450-800MHz Reference Design

Figure 2 – Load impedance as seen by AP603 with output matching network tuned from 400MHz to 800MHz with 50Ω and 25Ω ports. As shown in Figure 3, S11 is for the 50Ω case and S22 is for the 25Ω case.

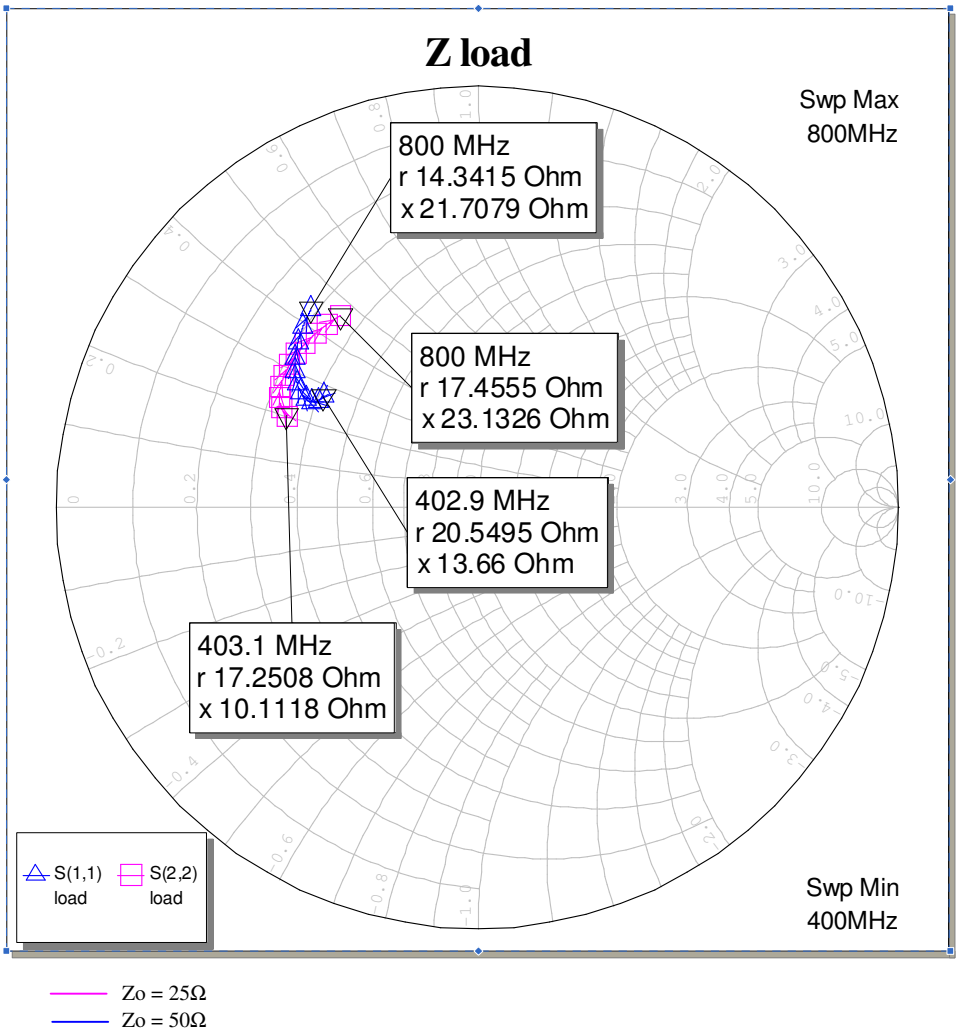


Figure 3 – AP603 Output Matching Network with Zo = 50Ω and 25Ω

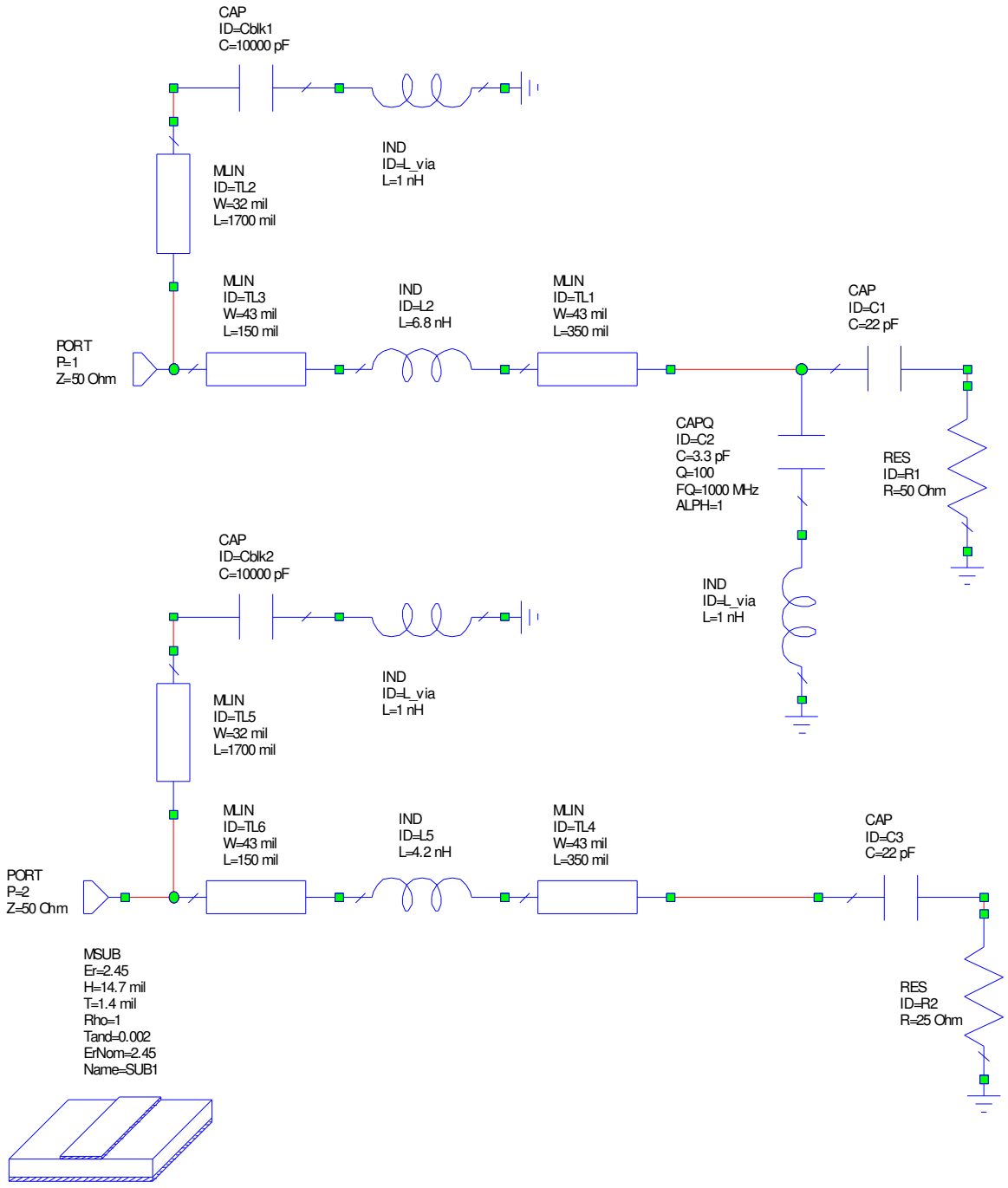


Figure 4 – AP603 with Input and Output Matching for 400 – 800 MHz

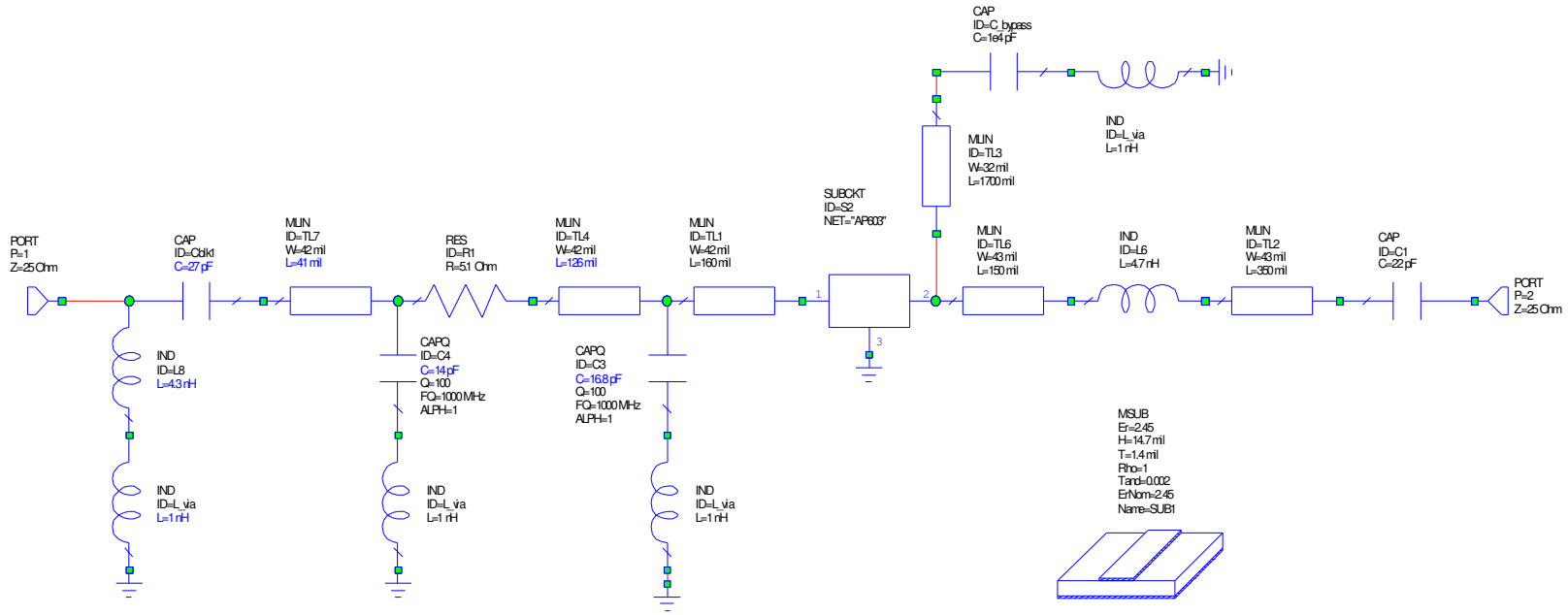


Figure 5 – S-parameters with Input Matching Network Tuned for S11 < -10dB and Flat Gain

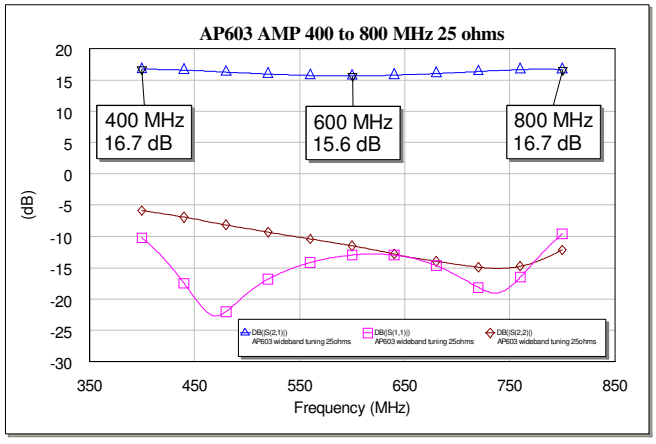


Figure 6 – Push-Pull AP603 AWR Simulation Schematic

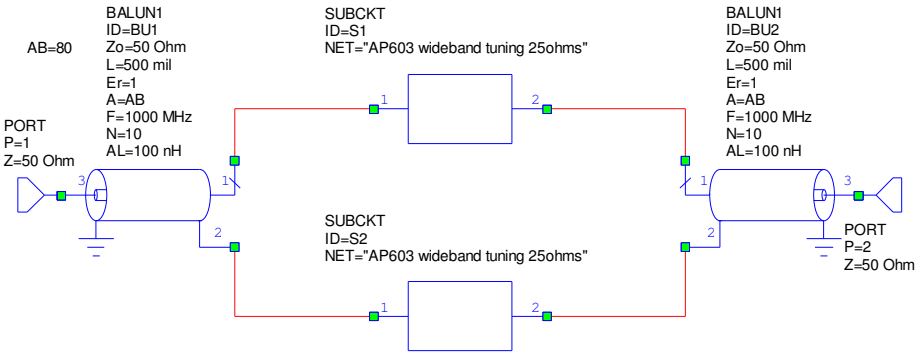


Figure 7 – Simulated Small-Signal Performance in Push-Pull Configuration

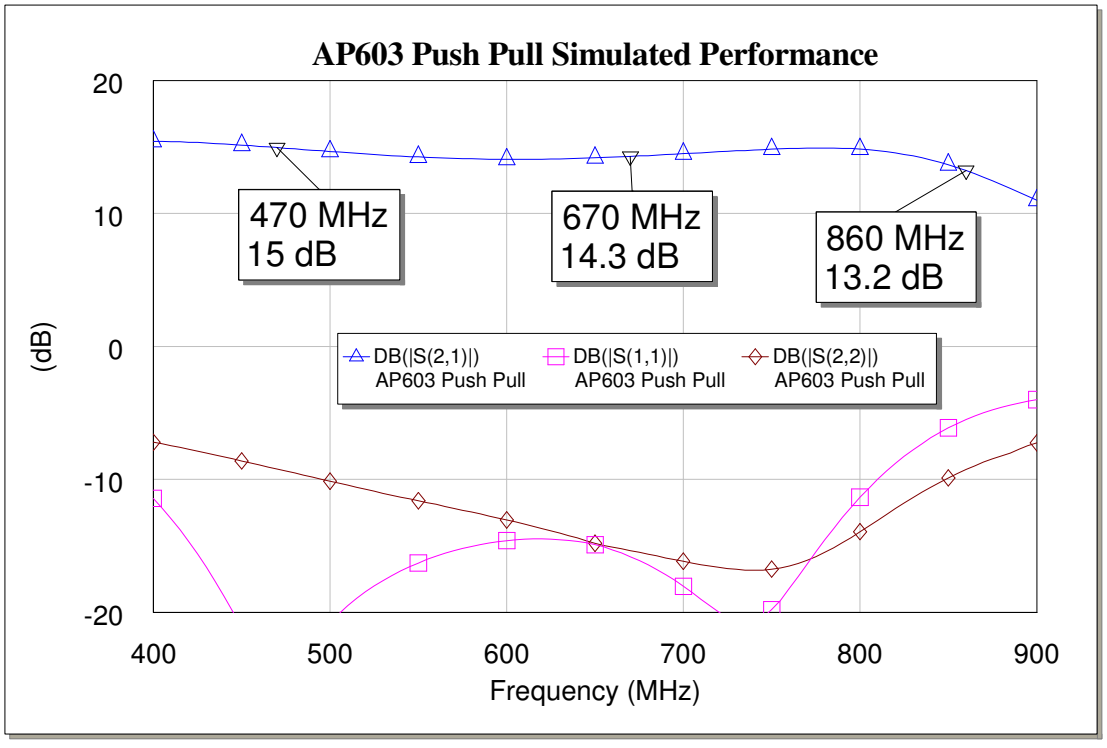
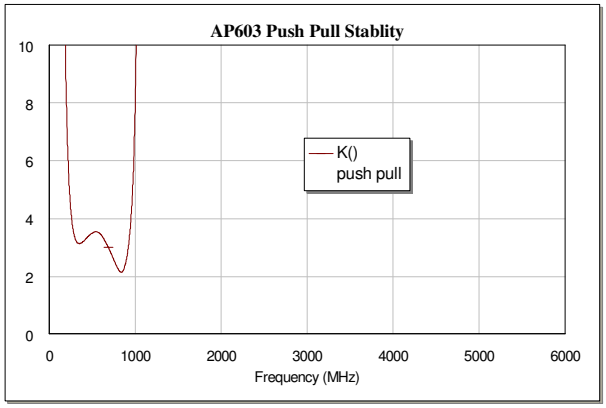


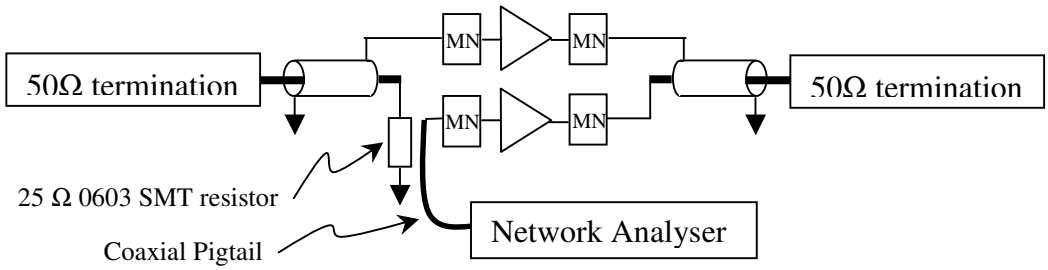
Figure 8 - AP603 Push-Pull Simulated Stability



Matching Network Measurement-Based Tuning Method

Subsequently, an evaluation board was fabricated and tuned based on measurements. The method for tuning the input matching network involved biasing both amplifiers and using a 'pig-tail' co-axial line to measure the input impedance of one of the input matching networks with the unbalanced terminal of the balun terminated to ground with a surface mount 25Ω resistor (Figure 9). Note, the network analyzer has Zo = 50Ω and this introduces an error to the measurement, but this technique is still useful for matching the amplifier. When tuning, of course, component values should be changed in both amplifier matching networks at the same time. A similar technique can also be used to measure the load-line, or output return loss.

Figure 9 - Input Impedance Measurement using a 'Pig-tail'



AP603 Push-Pull Reference Design Schematic

The AP603 push-pull reference design (Figure 10) uses Anaren 3A325 baluns (with a power rating of 275W) and 0603 surface mount components for the matching networks. Many inexpensive surface-mount baluns such as a M/A-Com ETC1-13-1 are available, but are only rated to 1W. For an amplifier with a P1dB of 42 dBm and a saturated Pout in the approximate range of 44-45 dBm, a balun with a power rating of at least 50W is required. The design of the matching networks has already been discussed.

Bias Circuit Description

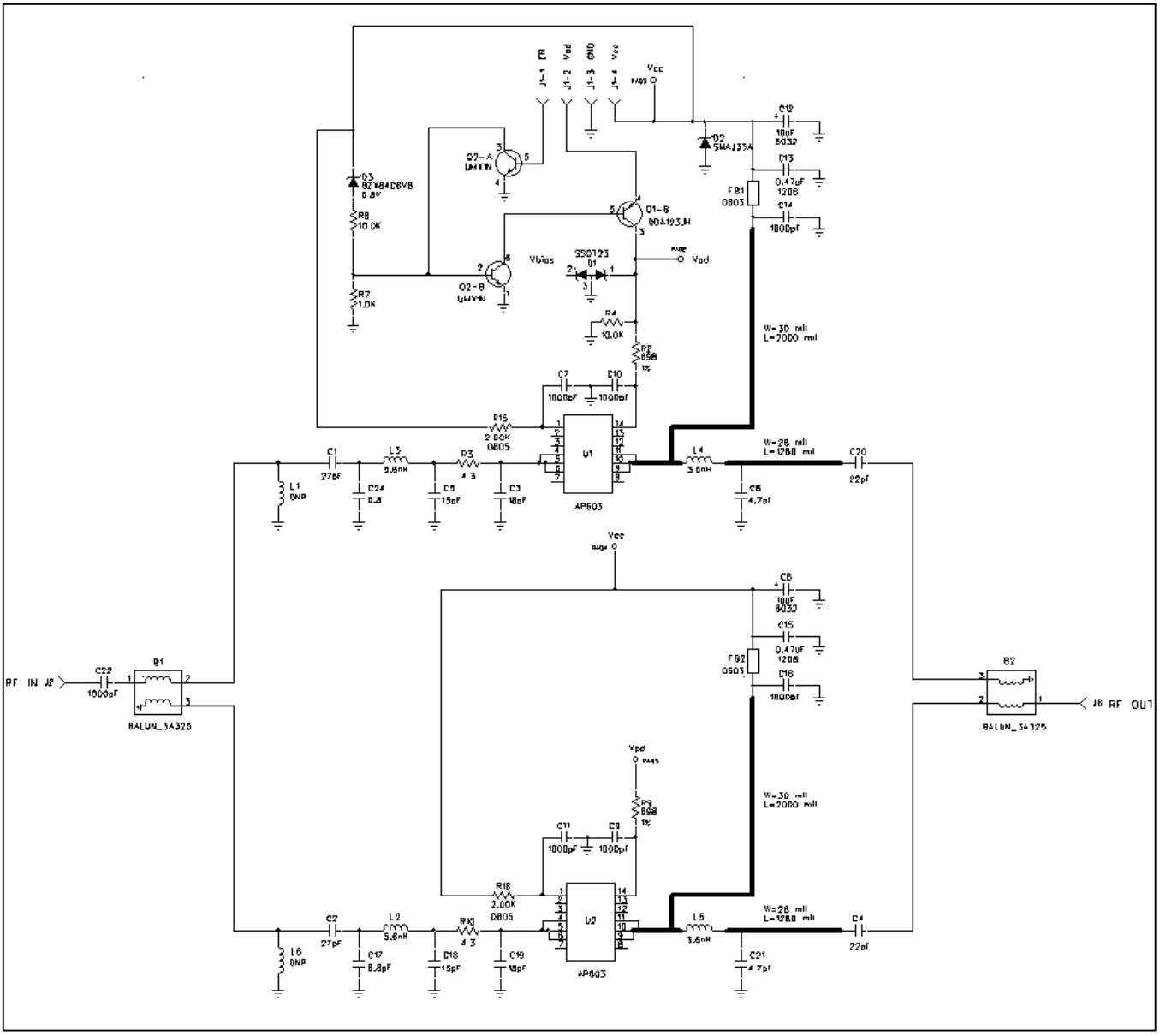
The AP603 features an internal active bias circuit. The Vpd (power down) pin (pin 14) is used to supply a reference current to the bias circuit. The pin 1 provides bias to an internal current buffer for the bias circuit. This bias is provided using Vcc (28V) dropping through a 2K resistor (R15 and R18). The Vcc pins (pins 9, 10 and 11) supply bias to the collector of the RF device. HBT power amplifiers can use emitter resistive ballasting to mitigate thermal runaway. For this circuit, Vpd must be shut off before Vcc because with Vpd biased Vcc will draw a small amount of current (approx 30mA) when Vcc is less than 15V

The AP603 push-pull reference design draws bias voltage through Vcc pin (28V) to ensure bias is not applied to the pin1 before the Vcc pin. The trade-off is efficiency versus simplicity. Ibias is approx 8mA for the AP603. The bias sequence circuit allows Ibias to be sourced from 28V.

Q1-B acts as a PNP switch to removes Vpd to the device when Vcc is not present. Q2 controls the reference current to Q1-B. In case of no supply on Vcc, Q1-B switch shuts off and therefore, no current on Vpd.

AP603 can be toggled ON-OFF by using the ENABLE_N pin. This pin can be controlled by a 3.3V (2.5 to 5V compliant) logic device such as a microcontroller. ENABLE_N is used to control the reference current to Q1-B through Q2. AP603 can also be switched on-off using Vpd (power down) pin.

Figure 10 – AP603 Push-Pull Reference Design Schematic



Board Substrate: FR4; Substrate thickness: 21 mil; εr = 4.2

Bias Feed Line: Width = 30 mil, Spacing = 35 mil;
50 Ω trace: Width = 39 mil, Spacing = 50 mil

Board Layout

The evaluation board uses 21mil thick FR4 (εr = 4.2). The 50Ω traces are 39mil wide with 50mil spacing to the top-layer ground. The bias feed is 30mil wide with 35mil spacing to the top-layer ground. Vpd, Vbias and Vcc are provided to the lower amplifier using backside jumper wires.

Figure 11 – AP603 Push-Pull Evaluation Board Showing Vpd and Vcc Jumper Wires

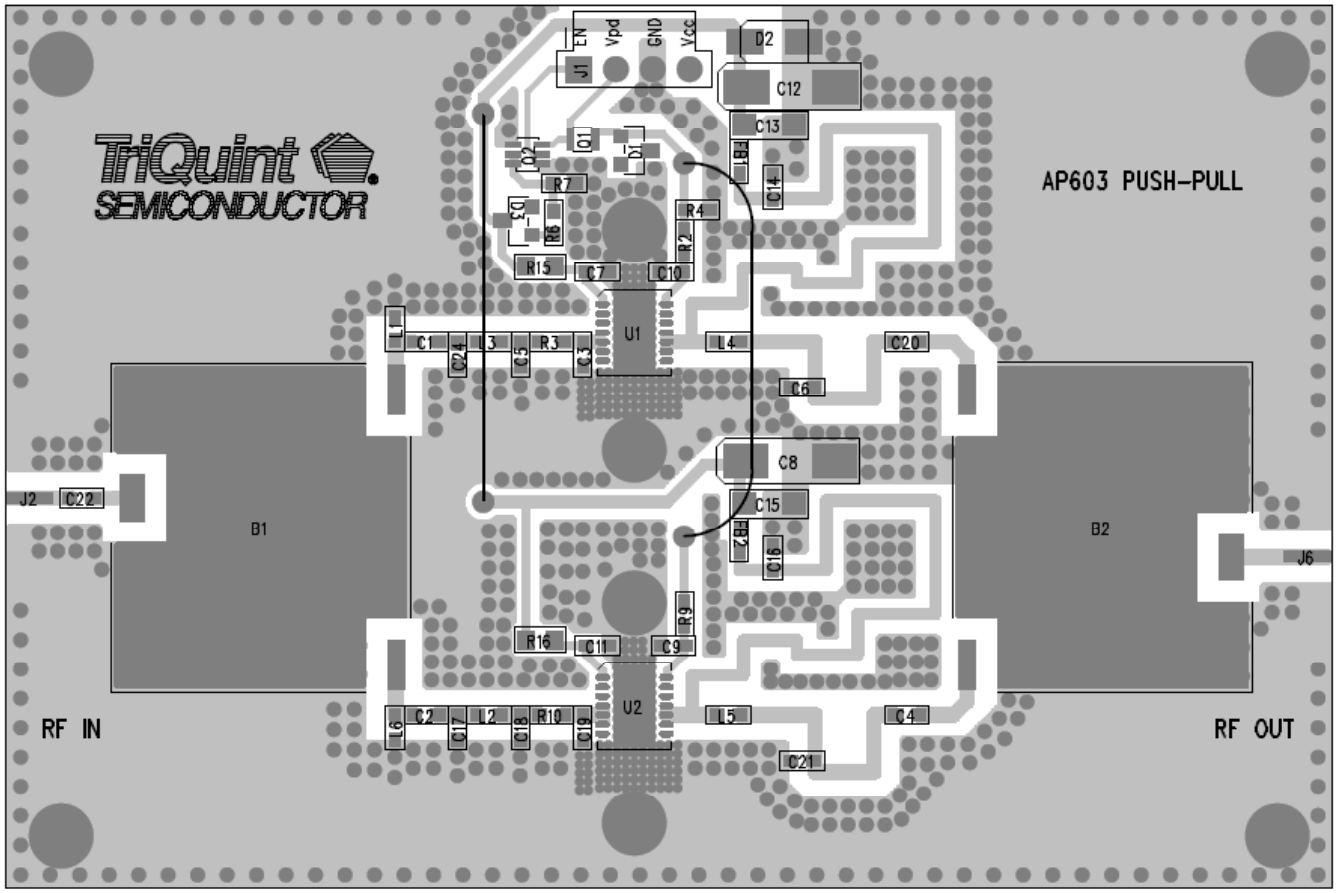
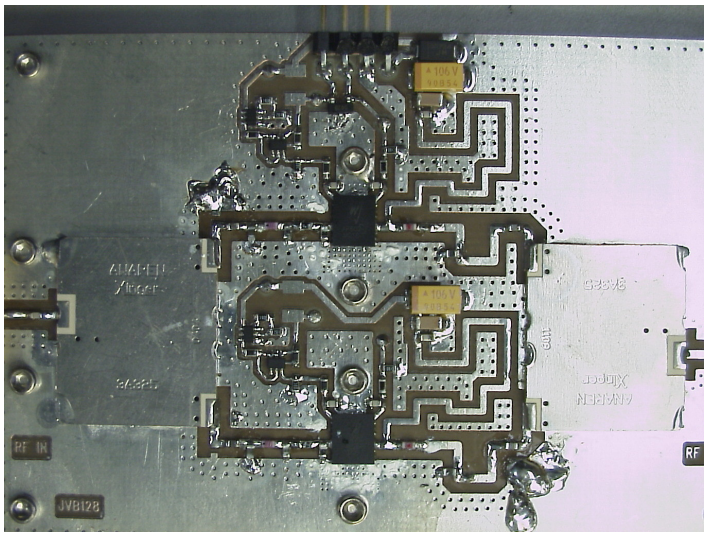


Figure 12 – Picture of Assembled PCB



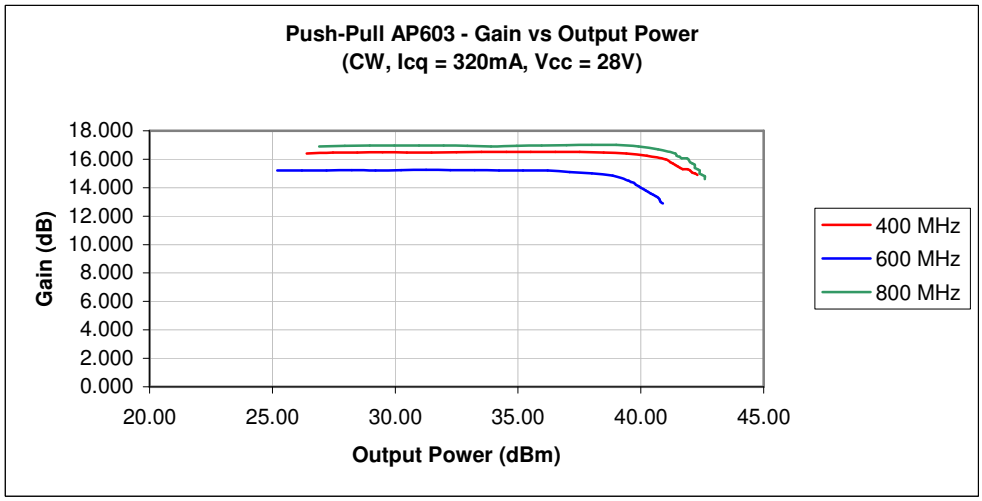
Assembled Board Picture is for the Rev0 board. Substrate: FR4; Substrate thickness: 21 mil; εr = 4.2

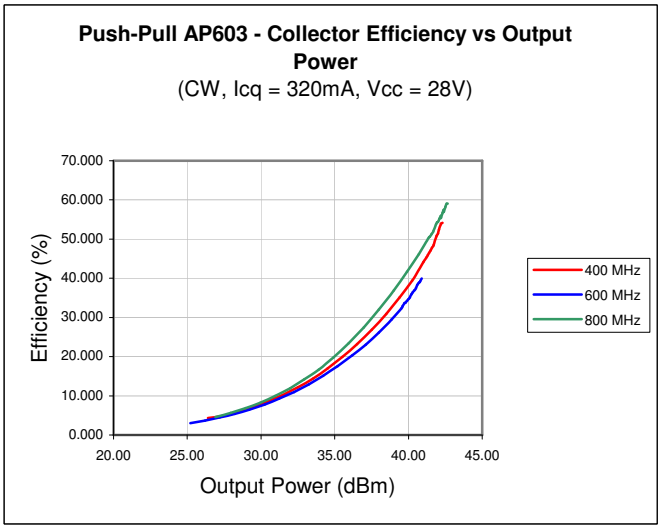
Bill Of Material

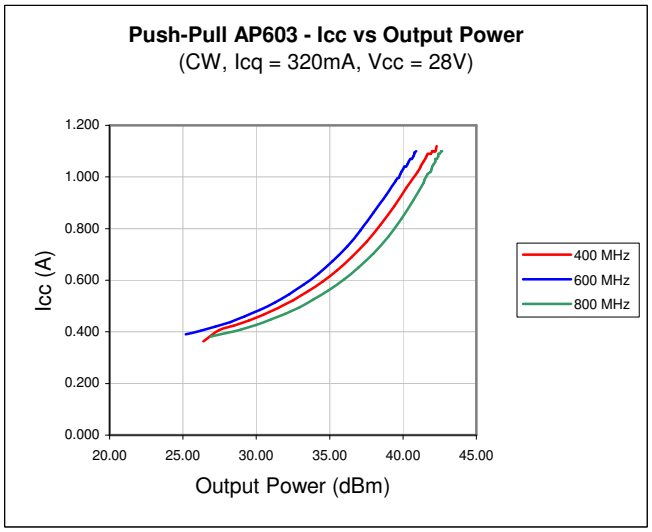
Item No.	Ref Des	Value	Part Style	Size
1	U1 U2	AP603-F	DFN14	5x6mm
2	B1 B2	na	Surface mount balun - Anaren 3A325	750mil x 890mil
3	Q1	na	Transistors –DDA123JH	SOT-563
4	C22, C16, C11, C9, C7, C10, C14	1000pF	Chip cap	0603
5	C5, C18	15pF	Chip cap	0603
6	C3, C19	18pF	Chip cap	0603
7	C1, C2	27pF	Chip cap	0603
8	C17, C24	6.8pF	chip cap	0603
9	C6, C21	4.7pF	Chip cap	0603
10	C13, C15	0.47uF	Chip cap	1206
11	C12, C8	10uF	Tantalum	6032
12	J2 J6	na	RF edge connector	na
13	D1	5V	zener diode	na
14	D2	33V	zener diode	na
15	D3	6.8V	zener diode	SOT-23
16	L4, L5	3.6nH	Wire wound chip inductor	0603
17	L1, L6	No load	Wire wound chip inductor	0603
18	L2, L3	5.6nH	Wire wound chip inductor	0603
19	R7	1.0k	Chip resistor	0603
20	R6, R4	10k	Chip resistor	0603
21	R15, R16	2.0k	Chip resistor	0805
22	R9, R2	698	Chip resistor	0603
23	R3, R10	4.3ohm	Chip resistor	0603
24	C20, C4	22pF	Chip capacitor	0603
25	FB1, FB2	22 ohm, 4A	Ferrite Bead	0603
26	J1	na	4-pin DC connector	na
27	Q2	na	Transistors - UMX1N	na

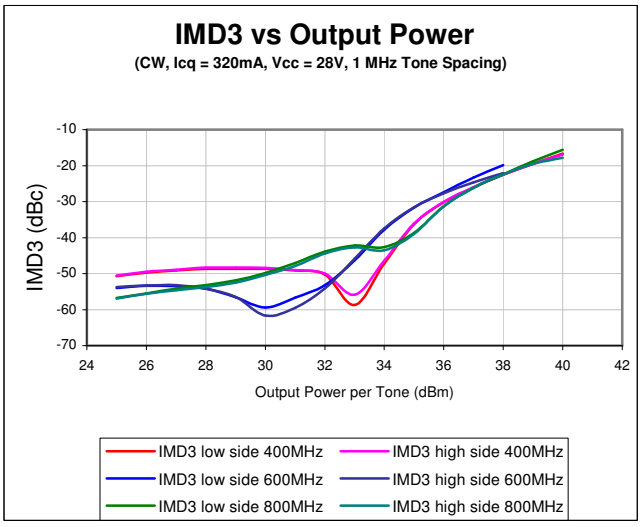
Measured Results

Figure 13 - Measured Performance vs Output Power









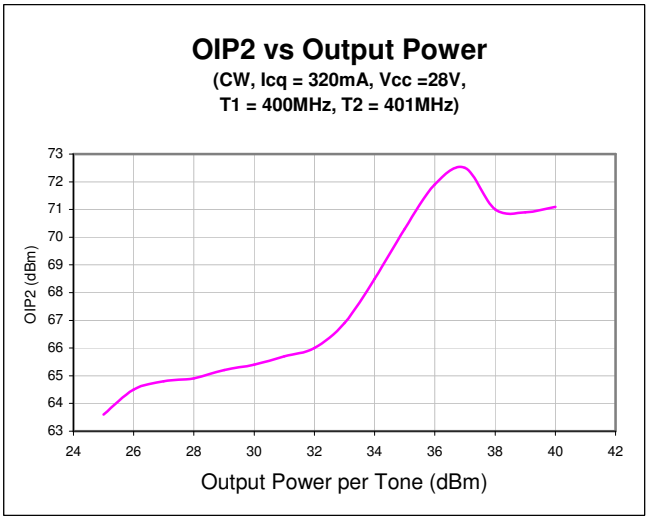


Table 1 - EVM vs Output Power and Frequency (802.16-2004 O-FDMA, 64QAM-1/2, 1024-FFT, 20 symbols and 30 subchannels)

Frequency (MHz)	Pout (dBm)	Icc (mA)	EVM (%)
400	34.7	635	2.5
600	33.7	695	2.5
800	34.8	570	2.5
400	36	660	4.3
600	36	713	6.6
800	36	596	5.3

Table 2 - P1dB vs Vcc and Frequency

Vcc	P1dB (dBm)		
(V)	400 MHz	600 MHz	800 MHz
18	40.8	40.6	39.2
28	42.3	40.5	42.8
32	41.8	40	43.3

Figure 14 - S-parameters with Vcc = 18V, 28V, 32V