PVD5870R

IQ Demodulator/Modulator

The PVD5870R is a direct conversion quadrature demodulator designed for communication systems requiring excellent linearity with low power consumption. The device is optimized for wide-band applications with RF inputs ranging from 200 – 3200 MHz.

Benefits of the component include excellent amplitude and phase balance, low conversion loss with low noise figure, very low DC offset, and low power dissipation. Intermodulation products IM2 and IM3 can be optimized through adjustment. RF, LO and baseband interfaces are fully differential. The baseband outputs of the device can interface directly to baseband amplifiers or low-pass filters.

The excellent linearity of the PVD5870R direct conversion quadrature demodulator can improve receiver dynamic range and significantly reduce bill of materials cost by eliminating the need for IF signal processing components.

General Features
- Operating RF Frequency:
  - 200 MHz to 3200 MHz
- Highest Linearity in class:
  - IIP3 +30dBm
  - IIP2 +70dBm adjustable
- Low insertion loss: 3.4dB @ 900MHz
- Noise Figure: 4.5dB @ 900MHz
- Phase Accuracy: 1°typical
- Amplitude imbalance: 0.05dB typical
- Low power consumption:
  - 900MHz RF, 23mA@3V, 33mA@1.8V
- Direct conversion
- Small PCB area and layout
- Low external component count
- Temp range: -40 to +85°C

Applications
- LTE, W-CDMA base station receivers
- Digital pre-distortion receivers
- RF-Identification (RFID)
- Wireless Local Loop (WLL)
- High-Linearity direct conversion receivers
- Point-to-point broadband radios

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Figure 1: PVD5870R Block Diagram
Contents

General Features ....................................................................................................................................................1
Applications ...........................................................................................................................................................1

**General Application as a Demodulator, device measuring circuit construction.** ........................................4

Goals of the design.................................................................................................................................................4

RF Input Section .....................................................................................................................................................5
  BALUN ............................................................................................................................................................................................... 5
  Attenuation Network (optional) ........................................................................................................................................................ 6
  DC Blocking Capacitors. ..................................................................................................................................................................... 6

LO Input Section ....................................................................................................................................................6
  BALUN ............................................................................................................................................................................................... 6
  DC Blocking Capacitors. ..................................................................................................................................................................... 6
  RF Chokes ...................................................................................................................................................................................... 6

Baseband Output Section .......................................................................................................................................6
  Output Transformer(s) ...................................................................................................................................................................... 7

Intermodulation Distortion Adjustment Section ......................................................................................................7
  CM Input............................................................................................................................................................................................ 7

Digital Control Section ............................................................................................................................................7
  nPD Input .......................................................................................................................................................................................... 7
  FBoost Input ...................................................................................................................................................................................... 7
  HLC Input ........................................................................................................................................................................................... 7

Power Supplies ......................................................................................................................................................7

Layout considerations .................................................................................................................................. 8

LO input considerations ............................................................................................................................... 9

Operation from Synthesizers having square wave outputs .............................................................................9

Operation using Single End’ed LO ..........................................................................................................................9
## Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Revision Description and Notes</th>
<th>Updated By</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rev A</td>
<td>07/27/14</td>
<td>Initial release</td>
<td>CM</td>
</tr>
<tr>
<td>Rev B</td>
<td>08/15/2015</td>
<td>Added LO section, filter use and single ended operation. Deleted NDA notice</td>
<td>CM</td>
</tr>
</tbody>
</table>
General Application as a Demodulator, device measuring circuit construction.

Probably the most instructive general application of the PV5870 as a demodulator is the measurement circuit found on our evaluation boards. By going through this circuit, we can become familiar with the elements required when applying the PV5870 to other conversion applications.

Goals of the design

Just as any design we started with application goals, a most of which are pretty standard for any RF demodulator application. Below is a list of those goals:

- Allow maximally accurate measurements of the figures of merit for the PV5870 as a demodulator;
  - RF operating bandwidth of 300 to 3000 MHz
  - BB bandwidth of 150KHz to 150 MHz
  - Insertion loss
  - Noise figure
  - Intermodulation products
  - I/Q phase and amplitude balance
  - Power consumption

- Optimize any or all of those parameters in the choices of surrounding components, and circuit layout.
- Exploration of various operating points.
- Maintain compatibility with industry standard test and measurement equipment.

A block diagram of one of these circuits is shown in Figure 2 Measurement Circuit block diagram below, followed a brief explanation of each circuit element’s function, and reason for choice.
RF Input Section

Following the signal from the RF input connector, we first create a balanced differential signal using a BALUN, followed by an optional resistive pad network, followed by DC blocking capacitors for the PV5870’s RF inputs.

BALUN

Given that our lab equipment is 50 ohms, single ended, an appropriate BALUN was chosen. The PV5870’s RF Input presents nominal 50 ohms differential impedance, so a 1:1 BALUN such as the Mini-Circuits T1-13M will suffice for most of the bandwidth of this application. For the upper end of the band an alternative BALUN, the T1-43M, which is compatible can be populated on the same printed circuit pattern.
Attenuation Network (optional)
For some measurements it may be advantageous to have a passive network to present a very low Q broadband impedance, or if you wish to increase the P1dB compression point above the PV5870’s normal compression point. Of course the pad will introduce an additional insertion loss and noise figure to the system; however the PVD5870’s low insertion loss and noise figure often allow this technique to be used, if needed.

DC Blocking Capacitors.
The PV5870’s RF inputs should track the baseband’s common mode voltage, which is 1.5V on the above circuit. So a DC blocking capacitor must be used on each input.

LO Input Section.
Following the Signal from the LO input we first create a balanced differential signal using a BALUN, then followed by DC blocking capacitors, and two DC return RF chokes for the PV5870’s LO input amplifier network.

BALUN
The factors in choosing the BALUN are very much like the RF path BALUN choice. Given that our lab equipment is 50 ohms, single ended, an appropriate BALUN was chosen. The PV5870’s LO Input presents a nominal 50 ohms differential impedance, so a 1:1 BALUN such as the Mini-Circuits T1-13M or T1-43M will suffice for this application. This is identical to the chosen BALUN for the RF input because our measurement application uses very low offset frequencies. If the target application used a higher offset frequency then one would need to choose a BALUN appropriate to the target LO frequency.

DC Blocking Capacitors.
The PV5870’s LO inputs require a localized DC return to ground which may not be adequately provided by the interface circuitry or test instruments. So a DC blocking capacitor must be used on each input.

RF Chokes
The LO input of the PV5870 is to a pair of common base amplifiers, and therefore need a DC path to system ground. The choice of the DC return components is driven by the need to have a high impedance at the LO frequency and a relatively low DC resistance. In the design above we chose a 27nH Coilcraft 0402CS inductor to meet this need.

Baseband Output Section
The In-Phase and Quadrature (I&Q) pins are differential outputs which are formed by successive energy samples of the incoming RF signal integrated onto the internal capacitors. The choice of impedance is a tradeoff between voltage gain, and linearity. A lower impedance will have less voltage gain, but will yield a more linear response, whereas a higher impedance will yield a higher voltage gain, but lower linearity. In the design of the evaluation boards we chose 125 ohms differential impedance, which yields Intermodulation products that give us ≥+30dBm IIP3, and ≥ +70 dBm IIP2 through most of the operating range, whilst maintaining a device insertion loss of ≤3.5dB up to about 1GHz.
Output Transformer(s)
For the evaluation circuit we needed to operate with our lab equipment which is usually 50 ohm, and single-ended. The choice of transformer was driven by the need to make extremely accurate A.C. measurements on the PV5870 device without the added uncertainty of active base-band signal processing components, and would allow us to make measurements in the range of \( 100 \text{KHz} \leq F_{\text{Meas}} \leq 150 \text{MHz} \). We chose a Coilcraft WB2.5-6TSL, which, with a 50 ohm load, will present 125 ohms to the PV5870, and by virtue of the center tapped primary, can also supply the 1.5V output common mode voltage to the IC. On the evaluation boards we also placed pads for passive elements to allow measurements at DC.

Intermodulation Distortion Adjustment Section

CM Input
This input sets the common mode bias condition on the I, and Q sample gates. The setting of this input can be varied to minimize the IM products at any given frequency. For applications which do not demand broadband operation, or the absolute minimum of IMD, this input can be set to a fixed voltage, usually in the range of 1.8 to 2.0 volts.

Digital Control Section
The PV5870 has three digital inputs which allow the control of general device operation

nPD Input
This input powers down the internal circuitry within the PV5870. When 0 volts is asserted on this pin the LO amplifier, and associated circuits are disabled.

FBoost Input
When asserted, this input causes a change to the pulse shape which is applied to the sample gates, to optimize their operation above \( \approx 2600 \text{ MHz} \). It is usually de-asserted for operation at lower frequencies.

HLC Input
When asserted, this input also causes a change to the pulse shape which is applied to the sample gates, in order to optimize operation at very high input signal levels. Asserting this pin will increase P1dB by about 6dB, with a corresponding increase in device insertion loss.

Power Supplies
The PV5870 requires three power supplies, 1.8 volt, 3.0 volt, and a 1.5 volt reference for the output common mode. The currents required for these supplies can be found in the PV5870 data sheet.
Layout considerations

To realize the full potential of the PV5870 careful attention must be paid the circuit layout topology. Good RF grounding techniques should be used, stray RF paths should be minimized, and desired RF paths should have a consistent impedance, and low loss. The PV5870 facilitates these practices by having the LO and RF routed into the IC package on opposite sides, with the Base Band outputs on a third side, therefore perpendicular to the RF and LO paths. Figure 3 PV5870 circuit layout below illustrates the way we applied the PV5870 IC to the evaluation PCB.

In addition to adequate grounding, the RF inputs, and the LO inputs are kept to minimal length, and guarded on each side and below to minimize stray paths, and to maintain consistent TLINE impedance. One area to pay particular attention to is the Base-Band output lines, these need to be well guarded, especially from the LO path to maintain the best possible IM2 performance. We chose to transit immediately to the bottom layer, which is on the opposite side of the RF reference plane, then route to the transformers, thereby minimizing the stray paths from the RF and LO inputs to the Baseband outputs.
LO input considerations

Operation from Synthesizers having square wave outputs

A number of synthesizers on the market have outputs which come from internal digitally based frequency dividers, and thus do not output a sinusoid. The 5870 requires a sinusoidal wave-shape in order to generate proper quadrature clocks for the sample gates. To get good phase accuracy the second and third harmonic of any such waveform needs to be down by ≥30dBc. A technique we have used with the 5870 for broad-band test equipment is to use COTS harmonic filters in the LO path. The filters are switched in or out of circuit depending on the operations frequency. Below is a schematic of the circuit we used in a RF arbitrary waveform generator to allow the use of a synthesizer which has square-wave outputs. The filters are switched by two control signals to select the frequency band of operation. Our application was for a laboratory grade complex RF modulator and was very rigorous with regards to phase accuracy, so to meet or exceed this over the operational bandwidth we used two ganged filters on some paths. Depending on your application two-ganged filters may not be necessary. Alternately low pass filters could be used, for such a filter the pass-band ripple can be traded away for cutoff steepness allowing the use of a more aggressive response such as Chebyshev.

Operation using Single End’ed LO

There may be instances where it is preferable to use a single end’ed LO instead of the recommended differential configuration. This can be done with the PV5870, by fixing one of the LO inputs to ground. If we refer our attention to Figure 3 PV5870 circuit layout, top in Red, selected Bottom traces in Cyan earlier in this app-note we can see the easiest way to do this to the reference circuit is to remove T2, then short across from pin 2 to pin 4 (L11 to C25 on the layout), then remove C24 & L4, replace L4 with a short to ground. The operation of the device is minimally affected as follows;

- The conversion loss is not affected.
- IIP2 is overall slightly lower, although at some frequencies its actually slightly higher.
- IIP3 is affected minimally.
- Phase Error is slightly higher through most of range.
- Amplitude balance is slightly worse through most of the range.
- Unit still operates “best in class” for I/Q demodulator.