

Biasing GaN on SiC HEMT Devices

DC biasing of GaN HEMT devices is very similar to GaAs pHEMT devices – they are both N-channel depletion mode transistors with 0.25um gate lengths. However, GaN transistors exhibit some behaviors that are not seen in the more mature pHEMT process.

Initially, the GaN device should be checked for its ability to pinch-off the drain current. The nominal pinch-off voltage for 0.25um power pHEMT devices is -1 volt (Vgs). At this voltage, the drain current is reduced to 0.5mA per mm of pHEMT periphery. To achieve this level of pinch-off in GaN devices the Vgs voltage is typically -4 volts. Due to differences in the materials and less precise control over the channel, the variation of pinch-off voltages is much greater in GaN than in pHEMT. This measurement is conducted with Vds = 2 volts for pHEMT and Vds=10 volts for GaN. Gate current leakage should be measured and should (ideally) be very low, below 100uA per mm of periphery (GaAs pHEMTs will typically be in the 1-10 uA/mm range). This is one of the challenges of the GaN material and related processing and many devices still exhibit gate leakage currents higher than this. The investigation is on-going to understand the causes of gate leakage and to find solutions to reduce it in the manufacturing environment. The relationship between gate leakage currents and RF performance and reliability has not been established so it's difficult to set an upper limit at this time. After confirming pinch-off, the drain voltage can be raised to the required operating voltage. It is expected that the drain current will rise somewhat as the drain voltage is increased. The power dissipation at this point is still very low and the device is off.

The gate voltage can now be increased (carefully) towards zero volts and the drain current observed as it increases toward the desired quiescent point. At a typical Vds voltage of 30 volts and a current density of 100mA/mm, the GaN device is dissipating 3 Watt for every mm of periphery whereas our typical GaAs pHEMT transistors will run at 0.75 to 1 Watt per mm and the GaN devices will dissipate even more power when driven into saturation. Even though SiC is a much better conductor of thermal energy compared to GaAs (both substrates are 100mm thick), the 3x higher power dissipation leads to hotter channel temperatures. The most difficult thermal problem with the GaN devices is that the thermal stack-up below the substrate hasn't changed from the solutions used with GaAs power devices. The best stack-up is the GaN/SiC substrate, attached with AuSn solder to a CuMo (or CuW or Cu-Mo-Cu metal clad) thermal spreader which is then attached to a much larger metal housing or plate. This attachment can be mechanical with thermal grease in the interface or a high thermal conductive epoxy or a solder joint (if the two dissimilar metals will allow for the CTE mismatch) or even a metal shim (Indium or similar). Through this stack-up 3 to 5 times more heat flows in virtually the same area as the GaAs devices. The result is that the temperature rise through this stack is 3 to 5 times greater and this results in much higher channel temperatures. Even operation at room temperature can be challenging unless careful thought is given to the thermal environment. The best test solution is to get the heat to a cold plate, cooled by liquid nitrogen or such, as quickly as possible (minimum thickness with the best thermally conductive materials).

At a stable operating point, assuming the device is also RF stable (no oscillations), it is often observed that the drain current will change over time with a fixed Vgs voltage. This is called current drift, and the explanation is that charge is slowly filling in the traps (defects) in the semiconductor, often on the surface in the HEMT channel. This changes the intrinsic Vgs voltage and therefore the drain current. The gate voltage can be adjusted to reset the drain current but it can continue drifting after this change. Application of a large RF signal seems to fill the traps quicker and less drift is observed after the RF signal is removed. Under large RF signal excitation, the drain current increases to the proper level for maximum output power and efficiency.



Changes in the DC characteristics over temperature have also been observed, as expected. The pinch-off (or threshold) voltage becomes more negative with increasing temperature. Transconductance and IDSS reduce with temperature. Breakdown voltage, whether two terminal (gate-drain) or three terminal (gate-drain and drain-source), reduces with increasing temperature and has more variability. Gate leakage current also increases. Typical gate-drain breakdown voltages are around 90 – 100 volts at room temperature. Testing is stopped at 80 volts, with -6 on the gate, and the drain current is recorded, instead of testing all the way to the breakdown voltage. With all these variables and interactions, the change in drain current vs. temperature depends on the starting point. At low current densities, 20 to 50 mA/mm, the current is likely to increase with temperature whereas at higher currents, 100 to 200mA/mm, the opposite is true – current decreases with temperature increases or is fairly constant. This behavior is more difficult to observe if the drain current is drifting at the same time. Low current densities are often chosen for GaN devices to minimize the power dissipation but this will be at the expense of more variability due to Vgs being closer to the pinch-off voltage.

Appendix

The following graphs show examples of drain current drift, effects on quiescent current of stimulating the device with RF at a level to compress the amplifier significantly, and drain current as a function of temperature both before and RF stimulation. All tests were performed on the same physical device.

DC Current drift TGF2023-05 [wafer 0935205-02]

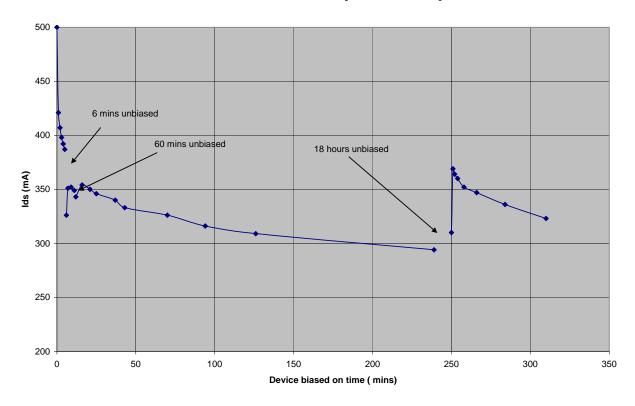


Figure 1



Figure 1 shows an example of DC current drift measured for a freshly assembled amplifier. The quiescent point was set initially to Ids=500mA (100mA/mm) with -3.6V gate voltage, and the drain current was observed to decrease initially with a high slope, which then decreased over time. After 5 minutes of continuous operation device was pinched off for 6 minutes after which the gate bias was reset to -3.6V. After a further 3 minutes of continuous operation the device was pinched off for 60 minutes, after which the gate bias was reset to -3.6V. When the gate bias was reset, the drain current was initially lower than expected but recovered to the expected value shortly after, attributed to the device warming up.

No significant recovery in drain current occurred during the 6 and 60 minute periods of pinched off state. After approximately 240 minutes of continuous operation, the drain voltage was set to zero and then the gate bias set to zero, for a period of 18 hours. After reinstating gate and drain bias, the drain current had recovered to some extent, after which it continued to decrease over time.

The amplifier was then left unbiased for a period of 10 days after which it was retested. The results are shown in Figure 2, and it can be seen that the drain current recovered only by a small amount, and the drift rate was slow.

Baseplate temperature =20 deg C u.o.s wafer 0935205-02 400 350 300 250 200 150 100 50 0 10 15 20 40 Time (mins)

Ids changes (Time) for 5mm GaN discrete (Vds=30V, Vgs=-3.60V)

Figure 2

The baseplate temperature was held at 20C (+/- 1) for the duration of these drift tests.

The effect of changing baseplate temperature from 20-55 C was then investigated (on the same device) and the results are shown in Figure 3. Drain current increased by about 30%. After returning to 20C



baseplate, the current had reduced slightly, which is attributed to further current drift, with some possible acceleration owing biasing at elevated temperature.

Baseplate temperature =20 dea C u.o.s wafer 0935205-02 450 400 350 300 150 100 100 20 30 405 60 70 80 90 Time (mins)

Ids changes (Temperature) for 5mm GaN discrete (Vds=30V, Vgs=-3.60V)

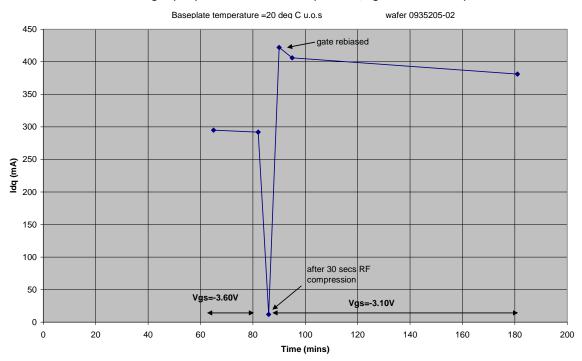
Figure 3

Next, the amplifier was driven with RF to about 3dB gain compression for 30 seconds. When the RF signal was switched off, it was observed that the quiescent drain current had dropped to a very low value, and the gate bias was readjusted to give Idq~400mA (gate voltage -3.1V). The results are shown in Figure 4. A small amount of residual current drift was then observed. On other samples, which had not been subjected to extensive DC bias beforehand, operation for a short period at RF compression reduced the amount of current drift very considerably. While extensive testing has not been carried out, it is believed that the effect of RF compression more or less permanently removes rapid current drift. Subsequent cycles of RF operation did not change the quiescent current significantly.

The last test performed on this sample was to look at the effect of baseplate tempature on Idq, and the results are shown in Figure 5. The drain current increased by about the same percentage as was observed prior to driving with RF.



lds changes (RF) for 5mm GaN discrete (Vds=30V, Vgs=-3.60 and -3.1V)



Figures 4 (above) and 5 (below)

Ids changes (Temperature) for 5mm GaN discrete (Vds=30V, Vgs=-3.1V)

