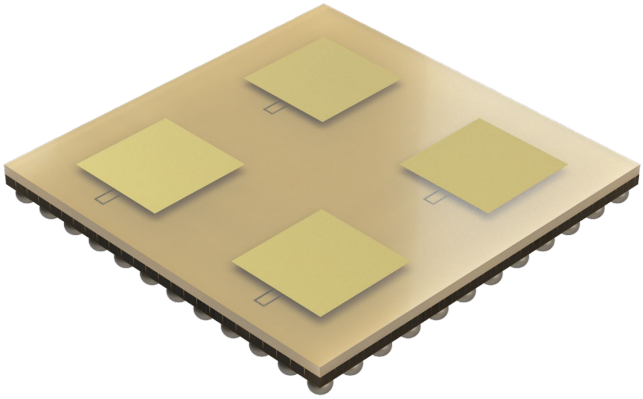
StingArray™
28GHz Integrated 2x2 Phased Array Module

Data Sheet ED2-0023

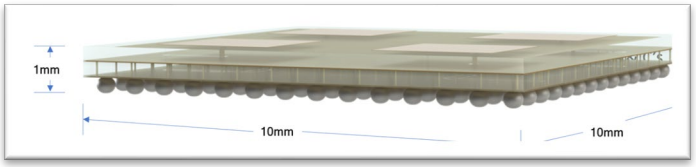
OVERVIEW

ED2's StingArray™-series Phased Array Module (PAM) is a System-in-Package. The StingArray™ PAM integrates 2x2 radiating elements with Renesas F5288 beamforming Half-Duplex transceiver for n257 band applications. The PAM minimizes loss and increases output power (EIRP +37dBm). The core IC has highly flexible gain and phase control on each channel to achieve fine beam steering and gain compensation between radiating channels. The PAM includes a standard SPI protocol that operates up to 65MHz with fast beam switching and fast beam-state loading.



APPLICATIONS

- 5G Phased-Array Antenna System, Beam Steering, and similar applications



FEATURES

- **EIRP +37 dBm**
- **+48.7 dB of total gain for transmit**
- **+34.4 dB of total gain for receive**
- 4 radiation channels
  - 100ns typical TX/RX mode switching time
  - 20ns typical gain and phase settling time
  - 1.4° (chip) typical phase error
  - 0.2dB typical RMS gain error
  - 30.5dB gain attenuation range
  - Integrated PTAT, PTAT2, and Bandgap generator
- Internal temperature sensor and power detector
- SMT package

BENEFITS

- **Reduces system complexity and cost**
- **Improves yields and manufacturability**

Power Supply

- Analog supply voltage: +2.4V to +2.6V
- Dedicated PA supply voltage: +2.4V to +2.6V and +3.0V to 3.3V

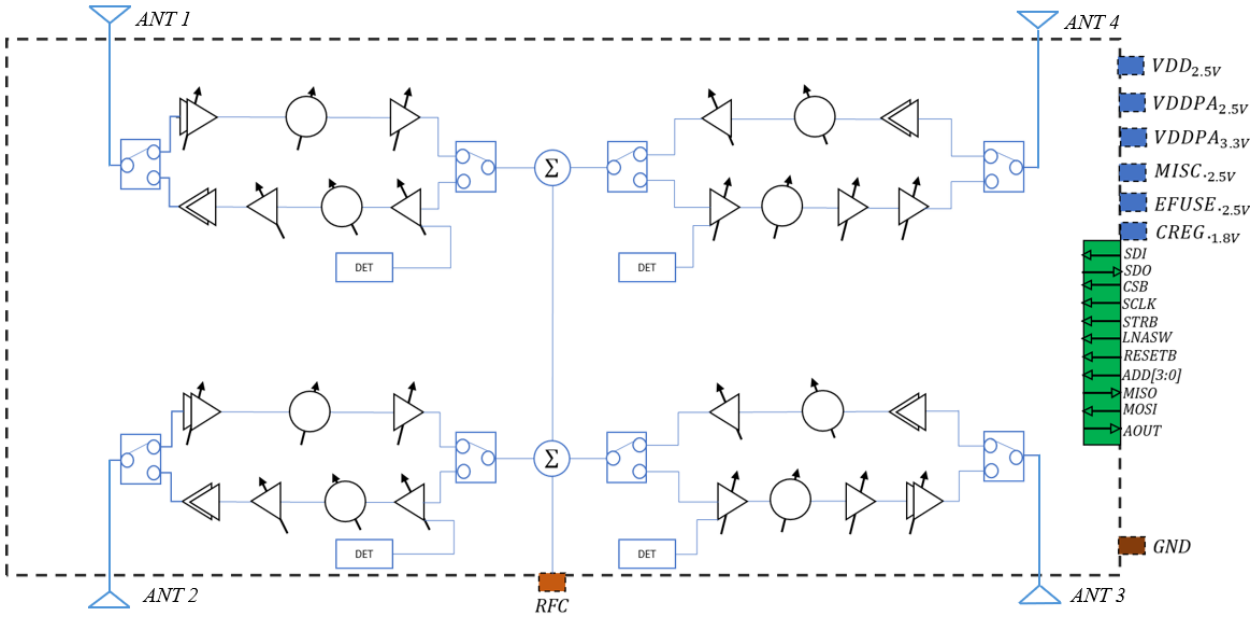
Mechanical Package

- 10 x 10 x 1.0 mm, BGA package

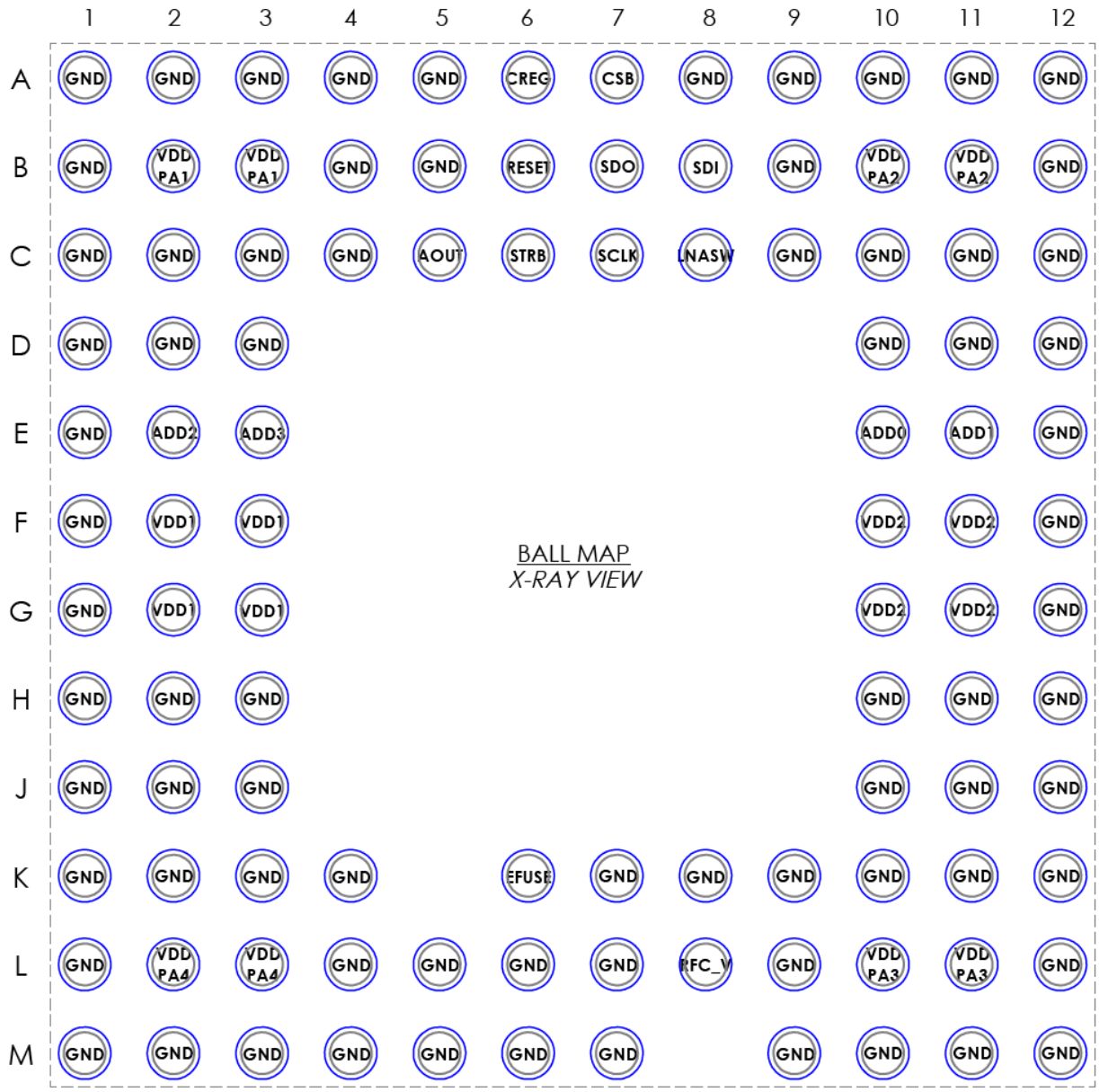
Temperature

- -40°C to +95°C operating temperature

Functional Block Diagram



Ball I/O Map (Top view through module)



Pinout

Ball Location	Type	Signal Name	Description
A1-A5	Ground	GND	Analog Ground
A6	Digital Input(PU)	CREG	Chip reset. 1 = operation mode, 0 = reset digital/memory to power-on reset default. Connected to CREG if not used.
A7	Digital Input (PU)	CSB	Chip select. 1.8V logic compatible.
A8-A12	Ground	GND	Analog Ground
B1	Ground	GND	Analog Ground
B2-B3	Analog Input	VDDPA1	2.5V/3.3V analog power supply for PA1
B4-B5	Ground	GND	Analog Ground
B6	Digital Input (PU)	RESET	Chip reset. 1 = operation mode, 0 = reset digital/memory to power-on reset default. Connected to CREG if not used.
B7	Digital Output	SDO	SPI data output. 1.8V logic compatible
B8	Digital Input (PD)	SDI	SPI data input. 1.8V logic compatible
B9	Ground	GND	Analog Ground
B10-B11	Analog Input	VDDPA2	2.5V/3.3V analog power supply for PA2
B12	Ground	GND	Analog Ground
C1-C4	Ground	GND	Analog Ground
C5	Analog Output	AOUT	Analog DC voltage test port for power detector or temperature sensor measurement. Output selection is controlled through a register setting. This pin can be grounded or left floating if not used.
C6	Digital Input (PD)	STRB	Digitally programmable strobe pin
C7	Digital input (PD)	SCLK	SPI clock. 1.8V logic compatible
C8	Digital Input (PD)	LNASW	RX Linearity mode direct control. 0 = set gain attenuation, 1 = max gain. Gain attenuation adjustable through register control setting. Should be connected to ground if not used.
C9-C12	Ground	GND	Analog Ground
D1-D3, D10-D12	Ground	GND	Analog Ground
E1	Ground	GND	Analog Ground

Ball Location	Type	Signal Name	Description
E2	Digital Input (PU)	ADD2	Chip Address bit 2.
E3	Digital Input (PU)	ADD3	Chip Address bit 3.
E10	Digital Input(PU)	ADD0	Chip Address bit 0.
E11	Digital Input(PU)	ADD1	Chip Address bit 1.
E12	Ground	GND	Analog Ground
F1	Ground	GND	Analog Ground
F2,F3	Analog Input	VDD1	2.5V analog power supply
F10,F11	Analog Input	VDD2	2.5V analog power supply
F12	Ground	GND	Analog Ground
G1	Ground	GND	Analog Ground
G2,G3	Analog Input	VDD1	2.5V analog power supply
G10,G11	Analog Input	VDD2	2.5V analog power supply
G12	Ground	GND	Analog Ground
H1-H3,H10-H12	Ground	GND	Analog Ground
J1-J3,J10-J12	Ground	GND	Analog Ground
K1-K4	Ground	GND	Analog Ground
K5,M8	Open	N/A	Ball pads removed per design
K6	Analog Input	VDD_EFUSE	EFUSE programming supply voltage pin for write operation (internal use only). For read operation, connect to VDD.
K7-K12	Ground	GND	Analog Ground
L1	Ground	GND	Analog Ground
L2,L3	Analog Input	VDDPA4	2.5V/3.3V analog power supply for PA4
L4-L7	Ground	GND	Analog Ground
L8	RF Input/Output	RFC_V	Vertical polarization common port
L9	Ground	GND	Analog Ground
L10,11	Analog Input	VDDPA3	2.5V/3.3V analog power supply for PA
L12	Ground	GND	Analog Ground
M1-M7,M9-M12	Ground	GND	Analog Ground

Absolute Maximum Ratings

Parameter	Symbol	Condition	Minimum	Maximum	Unit
Analog Supply Voltage	V_{DD}	-	-0.3	+3.0	V
PA Supply Voltage	V_{DDPA}	-	-0.3	+3.3	V
CSB, SDI, SCLK, STRB, LNASW, RESETB, ADD0, ADD1, ADD2, ADD3	V_{CTL}	-	-0.3	+2.1	V
TX Mode RF Common Port Input Power	P_{ABS_TX}	CW, 10s single event V_{DD} +2.5V, V_{DDPA} = +2.5V and 3.3V, T_{AMB} = +95°C	-	+15	dBm
RX Mode RF Channel Input Power	P_{ABS_RX}	CW, No damage for at least 2 hours V_{DD} +2.5V, V_{DDPA} = +2.5V and 3.3V, T_{AMB} = +95°C	-	+4	dBm
Maximum Junction Temperature	T_J	-	-	150	°C
Power Dissipation	P_D	-	-	7	W
Storage Temperature Range	T_{ST}	-	-40	+150	°C
Lead Temperature (soldering, 10s)	T_{LEAD}	-	-	+220	°C
ESD Rating - Human Body Model (Tested per JS-001-2012)	V_{HBM}	-	-	2500	V
ESD Rating – Charged Device Model (Tested per JESD-C101)	V_{CDM}	-	-	250	V

Electrical Characteristics

Parameter	Symbol	Condition		Min	Typical	Max	Unit
Logic Input High Voltage	V_{IH}			1.6	-	1.8	V
Logic Input Low Voltage	V_{IL}			0	-	0.3	V
Logic Input Current	I_{IH}, I_{IL}	For each input control pin		-50	-	50	uA
Logic Output High Voltage [1]	V_{OH}	I_{OH} = -2mA		1.35	-	-	V
Logic Output Low Voltage [2]	V_{OL}	I_{OL} = 2mA		-	-	0.45	V
2.5V Analog Supply Current & PA Supply Current	I_{VDD_2V5}	All 4 RX channels ON					mA
		All 4 TX channels OFF		-	448	565	
		All 4 RX channels OFF All 4 TX channels ON	NO RF Input	-	551	650	
			37.6 dBm EIRP	-	571.2		
TDD Switching Time	SW	RF Switch transition between TX and RX states		-	100	-	ns
		From Standby state		-	100	-	
Gain Settling Time	G_{ST}	97% settling time		-	20	-	ns
Phase Settling Time	PH_{ST}	97% settling time		-	20	-	ns
Phase Control Range	PH_{RANGE}	-		-	360	-	deg
Phase Control Resolution	PH_{RES}	6-bit control		-	5.6	-	deg
Temperature Sensor Accuracy	TEMP	After calibration [2]		-5	-	5	°C
SPI Clock Rate	SPI_{CLK}	-		-	-	65/95[3]	MHz

1. V_{OH} and V_{OL} parameters are simulated with an estimated load resistance of 1.7kΩ and load capacitance of 8pF.
2. For calibration procedure, refer to Power Detector and Temperature Sensor section
3. SPI write operations are rated up to 95MHz clock speed. Other SPI transactions, including read operation, are rated up to 65MHz clock speed.

Recommended Operating Conditions

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Analog Supply Voltage	V_{DD}	-	+2.4	+2.5	+2.6	V
PA Supply Voltage	V_{DDPA}	Default Power Mode	+2.4	+2.5	+2.6	V
		High Power Mode	+3.0	-	+3.3	
Operating Temperature Range	T_{AMB}	Ambient Temperature	-40	-	+95	℃
Operating Junction Temperature	T_J	-	-	-	125	℃
RF Frequency Range	f_{RF}	-	26.5	-	29.5	GHz
RF Pin Impedance	Z_{RF}	-	-	50	-	Ω

Electrical Characteristics - TX

Parameter/Condition	Specification
Frequency Range	26.5 – 29.5 GHz
Gain, *max gain setting*	42-47.5 dB Typ
Noise Figure, *max gain setting*	20.9 dB Typ
EIRP @ Output P1dB @ 1 ft (F_{RF} = 28GHz)	37.6 dBm
Output $IP3_1$	26.9/28.9 dBm Typ
3GPP-Compliant Linear Output Power *(5G-NR 400MHz 64QAM CP-OFDM, 120kHz sub-carrier spacing, output power with 3% EVM)*	14.5 dBm Typ
Adjacent Channel Leakage Ratio $(ACLR)_3$ *(5G-NR 400MHz 64QAM CP-OFDM, 120kHz sub-carrier spacing, at 3% EVM P_{out})*	-34 dBc Typ
Gain Control Range (G_{ATT_RANGE}) *monotonic vs control code*	29.2 dB Typ
Input Return Loss RL_{in}	6 dB max, 10 dB Typ
Power Detector Dynamic Range, PD_{RANGE}	-5 dBm min; 18 dBm max
Power Detector Accuracy, PD_{ACC}, Avg pwr vs process and voltage. Output Return Loss ≥ 3dB.	±1.2 dB
Reverse Isolation, ISO_{REV}, Maximum gain setting	37.2 dB
Channel-to-channel Isolation, ISO_{CH}, adjacent channels, maximum gain setting	36.8 dB

Electrical Characteristics - RX

Parameter/Condition	Specification
Single Path $Gain_1$ / maximum gain setting	16-20 dB 18 typ
Noise Figure / maximum gain setting	4.9 dB
Input P1dB / maximum gain setting	-27.9 dB
Input IP3dB / maximum gain setting, Pin -43dBm/tone, 100MHz/400MHz spacing	-20.3/-18.5 dBm
Gain Control Range (G_{ATT_RANGE}) / monotonic vs control code	15.5 dB
Gain Control Resolution (G_{RES}) / Gain mode = 0	0.5 dB Typ
RMS Gain Step Error ($G_{STEP-ERR}$)	0.09 dB Typ
Gain Flatness G_{FLAT}, 1GHz range at center	0.4 dB Typ
Gain Flatness G_{FLAT}, 1GHz range at band edges	1.6 dB Typ
Input VSWR RL_{IN}	2:1
Reverse Isolation, ISO_{REV}, Maximum gain setting	37 dB
Channel-to-channel Isolation, ISO_{CH}, adjacent channels, maximum gain setting	38.6 dB

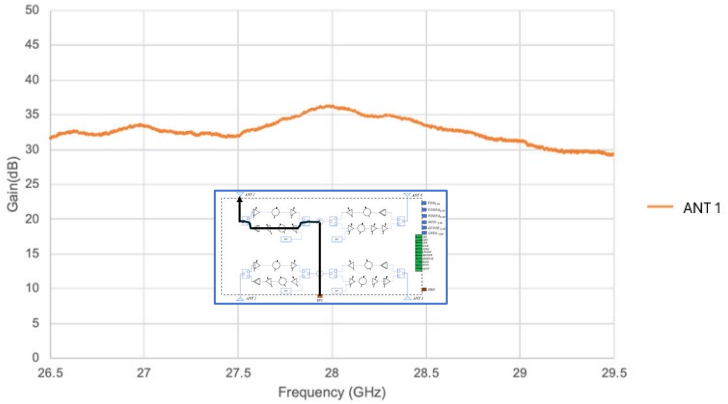
Notes:

1. Single path gain (SPG) is the S21 measured between antennas and RFC ports. For electronic gain (EG), 6dB division loss should be added to the SPG (EG = SPG + 6dB)

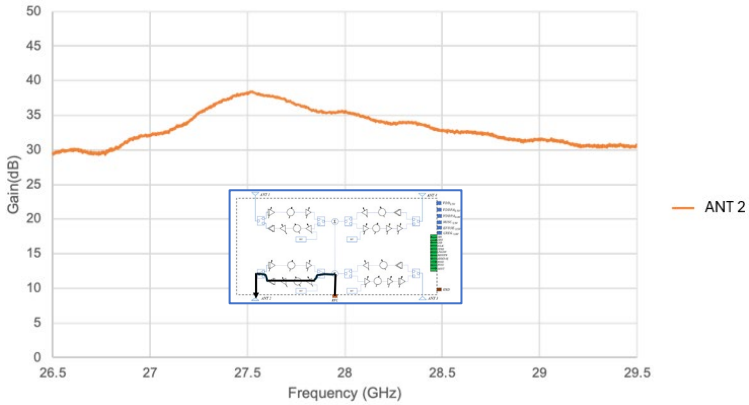
Measured Test Results

Transmit Data

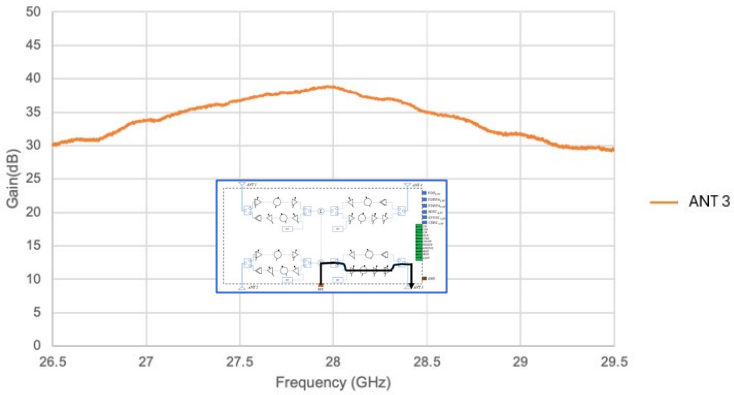
Transmit Channel (ANT 1)



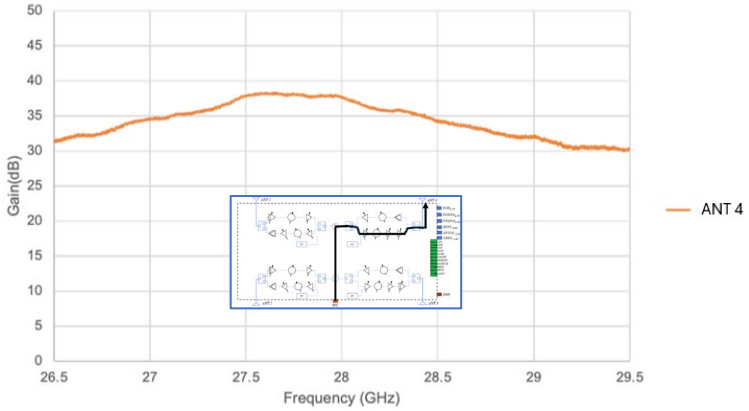
Transmit Channel (ANT 2)



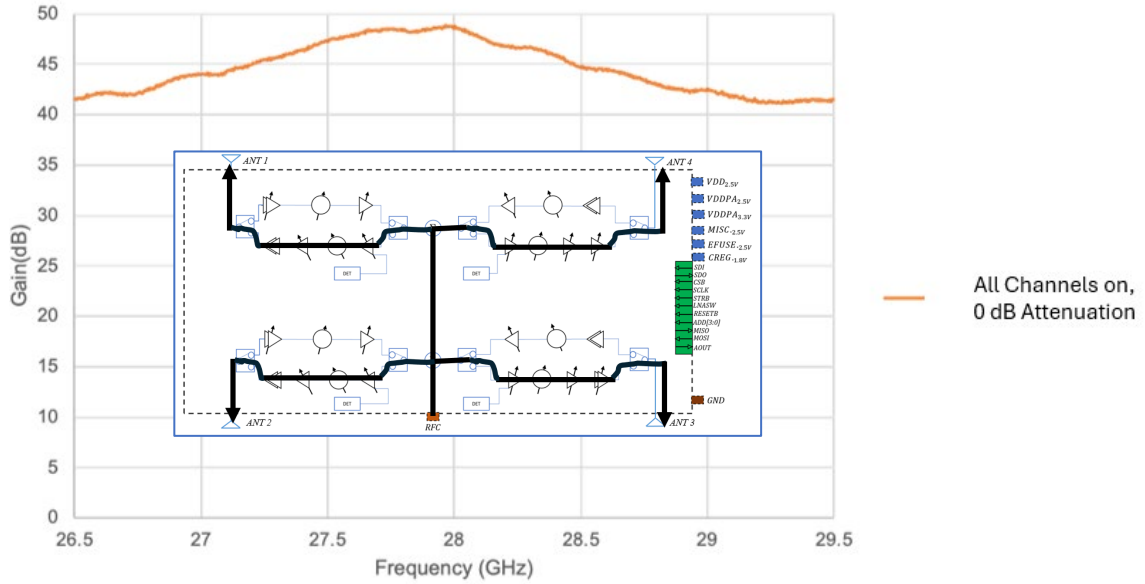
Transmit Channel (ANT 3)



Transmit Channel (ANT 4)

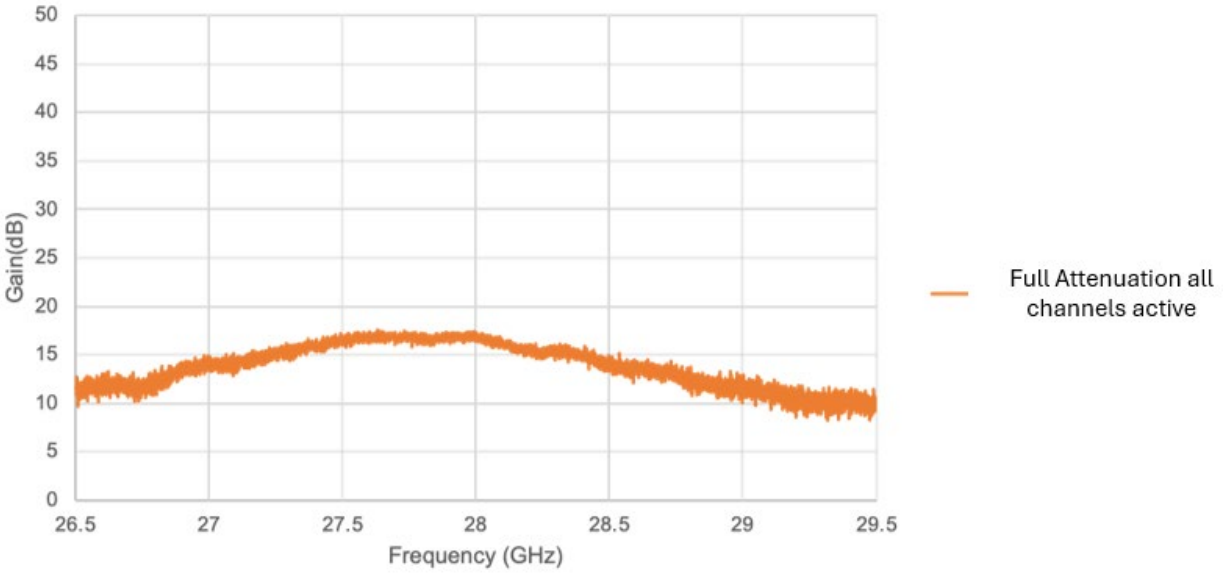


Transmit (All Channels)

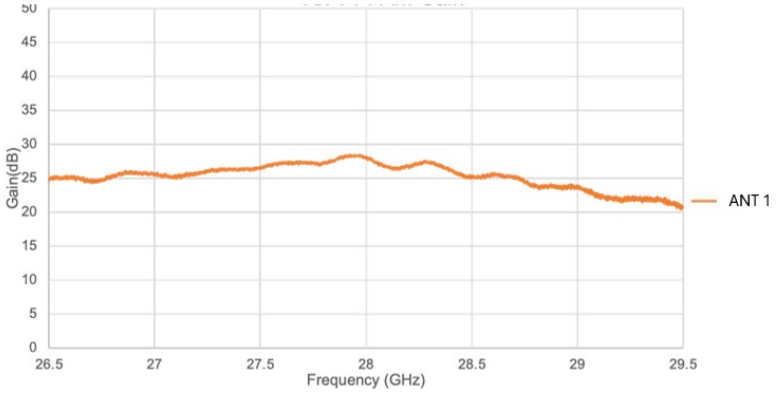


+28.7 dBm EIRP @ Pin -20 dBm 28GHz; PA Vias +2.5V

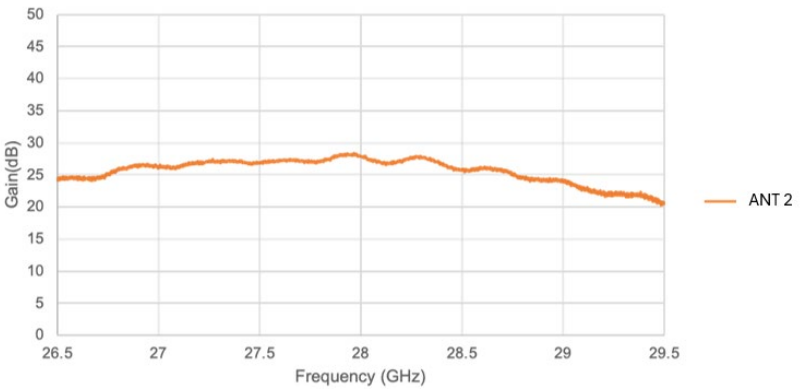
Transmit (Full Attenuation on All Channels)



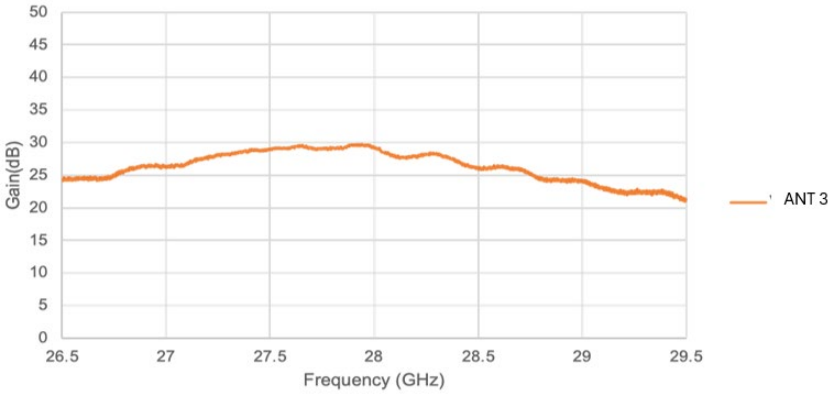
Receive Channel (ANT 1)



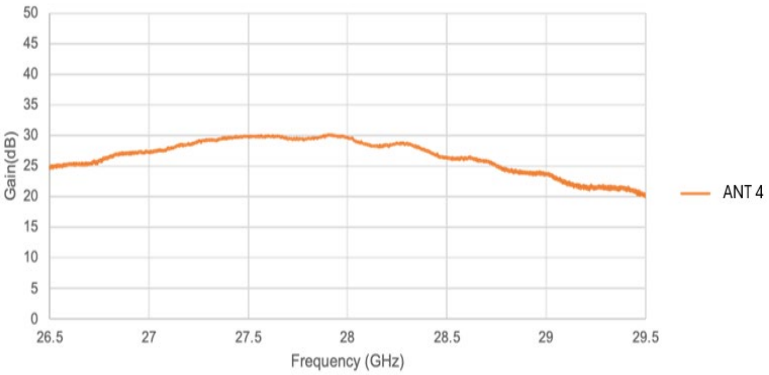
Receive Channel (ANT 2)



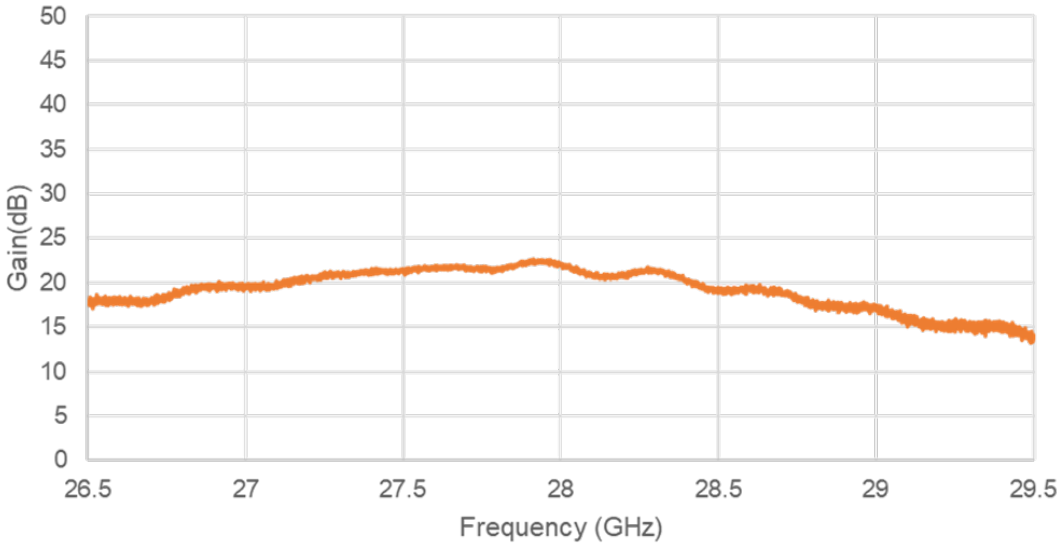
Receive Channel (ANT 3)



Receive Channel (ANT 4)



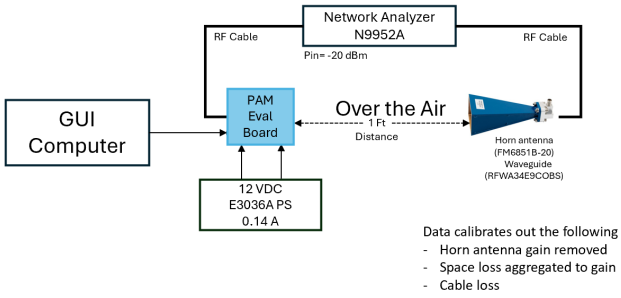
Receive Channel (All Channels, Max Attenuation)



Evaluation Board

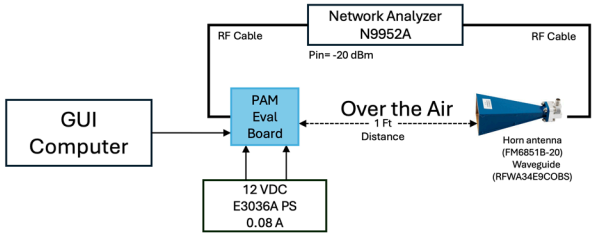
Setup

TRANSMIT



Data calibrates out the following
- Horn antenna gain removed
- Space loss aggregated to gain
- Cable loss

RECEIVE



Evaluation Board Images

PAM Module Eval Board

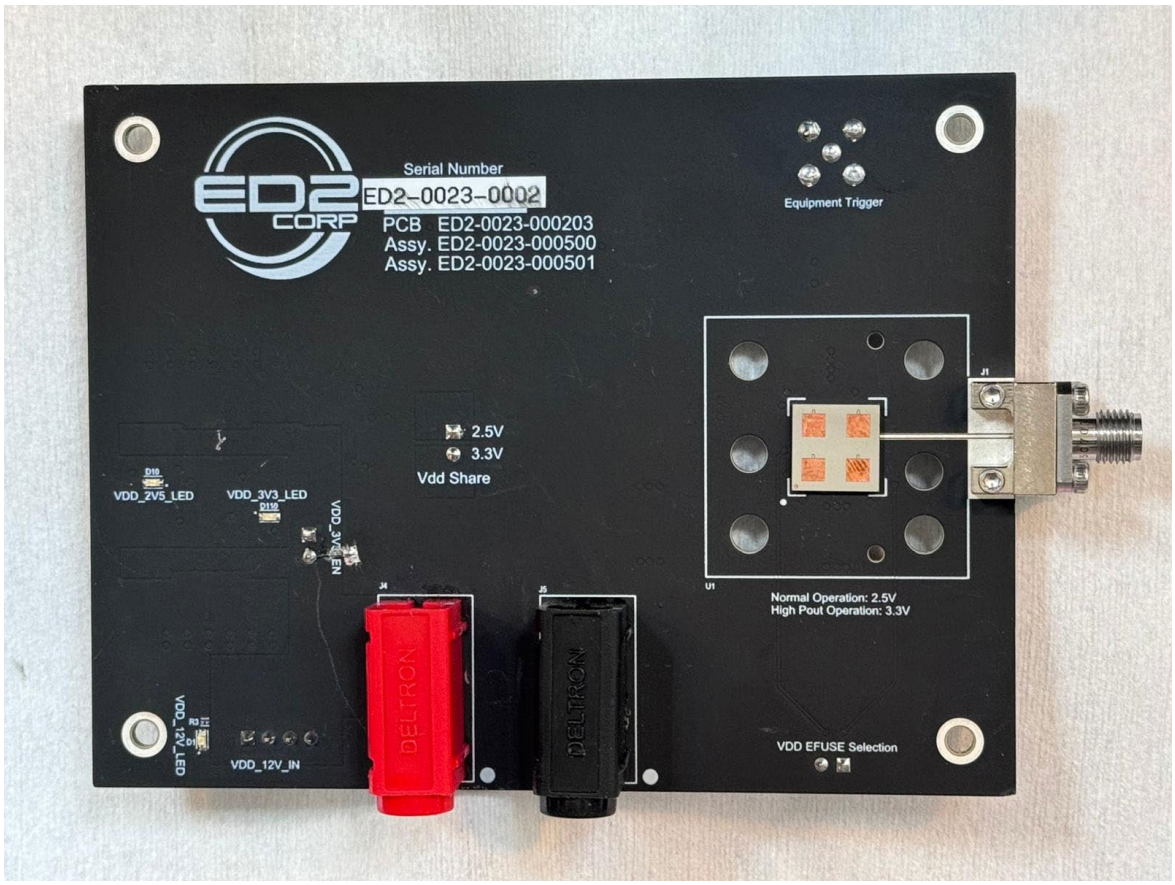


Figure 1. SN ED2-0023-0002

PAM Module Eval Board (bottom)

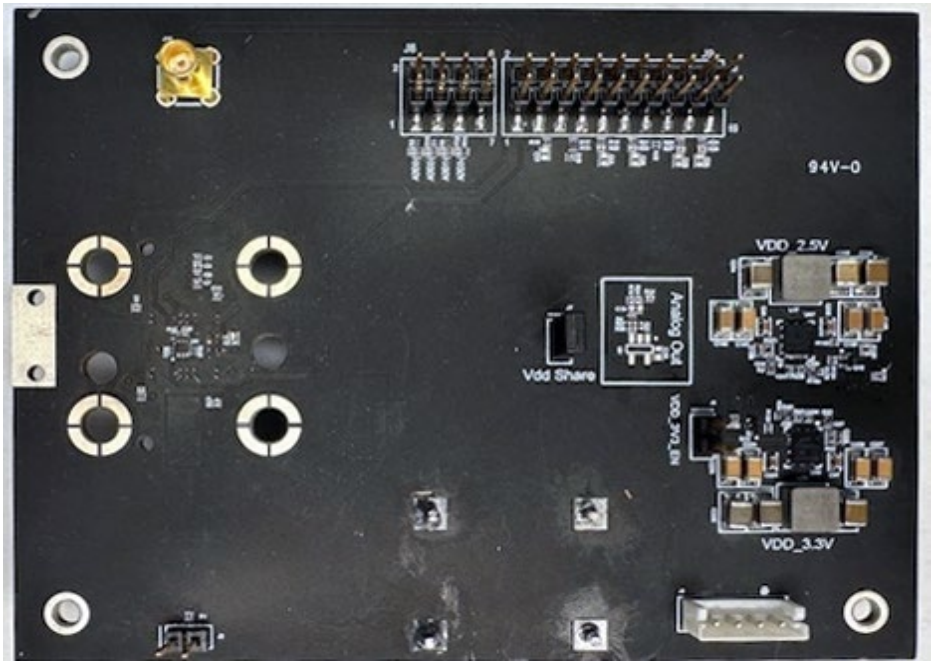


Figure 1. ED2-0023-0001 – bottom view

Figure 2.Digital Interface Board. ED2-0027-0003

Notes:
For more details on beamforming capabilities, please refer to F5288-Datasheet-v300 rev0.14 or the latest version from Renesas.

LNASW Control

The LNASW pin provides fast switching of the RX input-stage attenuator. Setting the LNASW pin low reduces the RX gain by the value set by RX_LinMode bits in the RXV_LNA registers to improve the linearity of the RX. To enable fast linearity switching through the LNASW pin, set the RX_LinMode_ExtPinEN bit in the RXV_LNA registers to '1'. If fast switching is not used (RX_LinMode_ExtPinEN=0), LNA gain attenuation is fully configured by the RXV_LNA registers. In this case, it's recommended to ground the LNASW pin.

LNASW Control Truth Table

RX_LinMODE_ExtPinEN	LNASW Pin	Linearity Mode
0	0	1 (RX_LinMode)
0	1	1 (RX_LinMode)
1	0	1 (RX_LinMode)
1	1	0 (Max gain)

VGA Gain Attenuation Control

TX VGA gain attenuation is controlled by the TXVn_SET[7:0] register to 29.2dB dynamic range of gain control for vertical channels. For TX gain control mapping and typical performance, see the following tables on the next page.

TX VGA Gain Attenuation Control: LUT

Gain Code	Gain Attenuation (dB)
255	0
251	0.5
247	1
243	1.4
239	1.9
232	2.6
228	3.1
224	3.6
220	4
216	4.5
213	5
208	5.7
207	5.9
201	6.4
196	7.1
193	7.5

Gain Code	Gain Attenuation (dB)
189	8
184	8.6
178	9.1
177	9.4
173	10
169	10.5
164	11.1
160	11.6
155	12
152	12.5
148	13.1
145	13.6
140	14
135	14.5
133	15
129	15.5

Gain Code	Gain Attenuation (dB)
123	16
120	16.4
114	17.1
112	17.5
106	18
105	18.3
101	18.9
97	19.4
94	19.7
90	20.2
85	20.9
80	21.3
76	21.8
72	22.2
68	22.8
64	23.3

Gain Code	Gain Attenuation (dB)
60	23.6
56	24
52	24.7
51	25
45	25.5
40	25.9
34	26.6
32	27.1
28	27.6
24	28
22	28.2
17	28.9
12	29.2

TX VGA Gain Attenuation Control: Typical Performance at 28GHz

Gain Code	Gain Attenuation (dB)	OP1dB (dBm)	OIP3 (dBm), 100MHz Spacing	OIP3 (dBm), 400MHz Spacing
255	0	19.2	26.9	28.9
239	1.9	19.2	25.3	27.5
224	3.6	19.2	24.3	26.2
207	5.9	19.2	23.0	24.3

RX VGA gain attenuation is controlled by the RXVn_SET[7:0] register to provide 15.5dB dynamic range of gain control for vertical channels. The RX channel also features a low-gain mode (RX_GAIN_MODE = 1) that can extend the overall gain control range up to 30dB. For RX gain control mapping and typical performance in high gain mode, see the following tables.

RX VGA Gain Attenuation Control in High-Gain Mode: LUT

Gain Code	Gain Attenuation (dB)
255	0
251	0.2
247	0.5
243	0.8
238	1
236	1.2
231	1.5
227	1.7
223	2
219	2.2
215	2.5
212	2.7
207	3
203	3.2
199	3.5
194	3.7

Gain Code	Gain Attenuation (dB)
191	3.9
188	4.1
183	4.4
179	4.7
176	4.9
171	5.2
168	5.4
162	5.7
159	5.9
156	6.1
151	6.4
147	6.6
142	6.9
138	7.1
135	7.4
131	7.7

Gain Code	Gain Attenuation (dB)
126	7.9
124	8.1
117	8.4
115	8.5
111	8.8
106	9,1
103	9.3
98	9.6
94	9.8
90	10
88	10.3
83	10.5
81	10.8
74	11
71	11.2
65	11.5

Gain Code	Gain Attenuation (dB)
62	11.7
59	11.9
58	12.2
49	12.5
46	12.7
45	13
41	13.2
36	13.5
32	13.7
29	13.9
21	14.2
20	14.4
16	14.7
10	15
7	15.1
3	15.5

RX VGA Gain Attenuation Control in High-Gain Mode: Typical Performance at 28GHz

Gain Code	Gain Attenuation (dB)	IP1dB (dBm)	IIP3 (dBm), 100MHz Spacing	NF (dB)
255	0	-27.9	-20.2	4.9
238	1.0	-27.9	-20.2	-
223	2.0	-28.5	-20.9	4.9
207	3.0	-29.1	-21.4	-
191	3.9	-27.9	-20.4	4.9
176	4.9	-29.0	-21.4	-
159	5.9	-27.9	-20.5	5.0

Phase Shifter Control

TX phase shifter is controlled by the TXVn_SET[15:8] register to provide 6-bit phase control with 360° dynamic range. Two bits are dedicated for process correction as shown in the "TX Phase Shifter Control" table.

TX Phase Shifter Control

D7 (MSB)	D6	D5	D4	D3	D2	Process Correction		Phase Shift (deg)
						D1	D0	
0	0	0	0	0	0	0	0	0
0	0	0	0	0	1	0	0	5.6
0	0	0	0	1	0	0	0	11.2
0	0	0	1	0	0	0	0	22.4
0	0	1	0	0	0	0	0	44.8
0	1	0	0	0	0	0	0	89.6
1	0	0	0	0	0	0	0	179.2
1	1	1	1	1	1	0	0	352.8

RX phase shifter is controlled by the RXVn_SET[15:8] register to provide 6-bit phase control with 360° dynamic range. Two bits are dedicated for process correction as shown in the "RX Phase Shifter Control" table.

RX Phase Shifter Control

Process Correction		D5	D4	D3	D2	D1	D0	Phase Shift (deg)
D7 (MSB)	D6							
0	1	0	0	0	0	0	0	0
0	1	0	0	0	0	0	1	5.6
0	1	0	0	0	0	1	0	11.2
0	1	0	0	0	1	0	0	22.4
0	1	0	0	1	0	0	0	44.8
0	1	0	1	0	0	0	0	89.6
0	1	1	0	0	0	0	0	179.2
0	1	1	1	1	1	1	0	352.8

RESETB Control

The device can be reset without power supply cycling, by toggling the RESTB pin from logic high to low. The RESETB pin needs to be asserted back to logic high for normal device operation. During the chip reset, the register contents return to the factory default values.

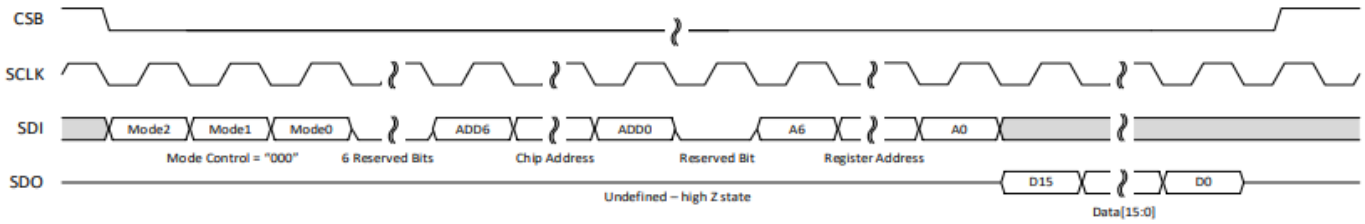
RESETB Control Truth Table

RESETB	State
0	Reset
1	Normal Operation

SPI Modes

Mode Control Bits	Mode of Operation	Description
000	LCL_REG_RD	Local Register Read
001	LCL_REG_WR	Local Register Write
010	GBL_LUT_WR	Global LUT Write
011	GBL_REG_WR	Global Register Write
100	GBL_FST_BM_STR	Global Fast Beam Steering
101	LCL_FST_BM_STR	Local Fast Beam Steering
110	LCL_LUT_WR	Local LUT Write
111	LCL_LUT_RD	Local LUT Read

LCL_REG_RD Timing Sequence



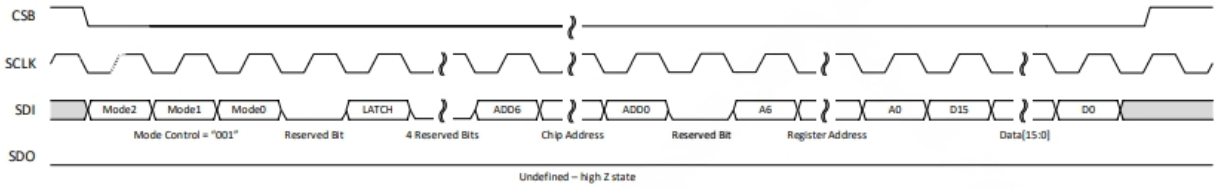
LCL_REG_RD Command Bit Sequence

Byte 1								Byte 2								Byte 3								Byte 4	Byte 5
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7...0	7...0
MODE			Reserved Bits					Chip Address								RES	Register Address							Data Read	
0	0	0	0	0	0	0	0	0	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0	0	A6	A5	A4	A3	A2	A1	A0	D15...D8	D7...D0

LCL_REG_RD Command Bit Definition

Byte	Bit	Description	Comment
1	[7:5]	Mode Control	For Local Register Read, mode=000
2	[6:0]	Chip Address	
3	[6:0]	Register Address	
4	[7:0]	Data Byte 1 - Data [15:8]	Master SCLK pulses and Data is received on the SDO line
5	[7:0]	Data Byte 2 – Data [7:0]	

LCL_REG_WR Timing Sequence



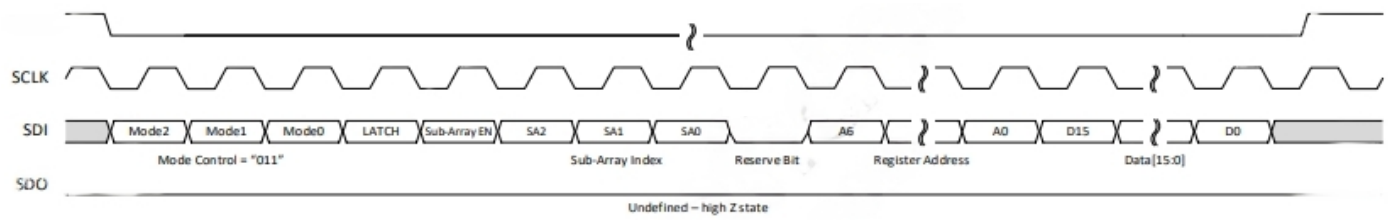
LCL_REG_WR Command Bit Sequence

Byte 1								Byte 2								Byte 3								Byte 4	Byte 5
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7...0	7...0
MODE			RF Load		Reserved Bits			Chip Address								RES	Register Address							Data Read	
0	0	1	0	Latch	0	0	0	0	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0	0	A6	A5	A4	A3	A2	A1	A0	D15...D8	D7...D0

LCL_REG_WR Definitions

Byte	Bit	Description	Comment
1	[7:5]	Mode Control	For Local Register Write, mode=001
1	[3]	Data Latch	0 = Data is written to buffer 1 = Data is written to buffer and register This bit also triggers the data latch for all other buffered registers on the chip
2	[6:0]	Chip Address	
3	[6:0]	Register Address	
4	[15:8]	Data Byte 1 – Data [15:8]	Data written on the SDI Line will be saved to buffer or register
5	[7:0]	Data Byte 2 – Data [7:0]	

GBL_REG_WR Timing Sequence



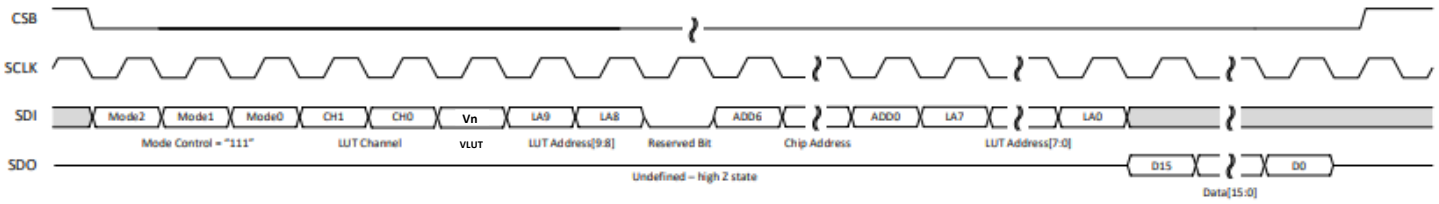
GBL_REG_WR Command Bit Sequence

Byte 1								Byte 2								Byte 3								Byte 4
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	15... 8
Mode			RF Load	Sub Array Enable	Sub Array Idx			RES	Register Address							Data								
0	1	1	Latch	SE	SA2	SA1	SA0	0	A6	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7... D0

GBL_REG_WR Command Bit Description

Byte	Bit	Description	Comment
1	[7:5]	Mode Control	For Local Register Write, mode = 011
1	[4]	Data Latch	0 = Data is written to the buffer 1 = Data is written to the server This also triggers the latch for all other buffered registers on the chip
1	[3]	Sub Array Enable	0 = Command executed on all chips 1 = Commands executed on chips with matching sub array
1	[2:0]	Sub Array Index	If SE is set, data is written only when this index matches with the chip's sub array index (stored in register 0x0)
2	[6:0]	Register Address	
3	[7:0]	Data Byte 1 - Data [15:8]	Data sent on the SDI line will be saved to the buffer or register
4	[7:0]	Data Byte 2 – Data [7:0]	

LCL_LUT_RD Timing Sequence



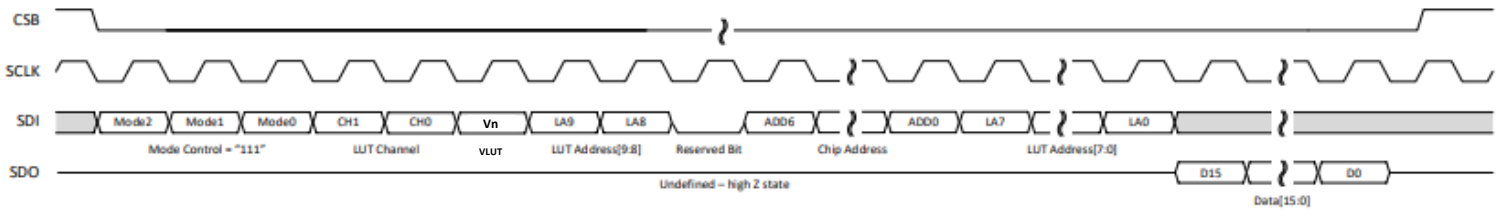
LCL_LUT_RD Command Bit Sequence

Byte 1								Byte 2								Byte 3								Byte 4	Byte 5
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7...0	7...0
MODE			LUT Channel		RES	LUT Address		RES	Chip Address							LUT Address								Data Read	
1	1	1	CH1	CH2	0	LA9	LA8	0	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0	LA7	LA6	LA5	LA4	LA3	LA2	LA1	LA0	D15...D8	D7...D0

LCL_LUT_RD Command Bit Description

Byte	Bit	Description	Comment
1	[7:5]	Mode Control	For Local LUT Read, mode = 111
1	[4:3]	Channel Select	Choose between CH0 – CH3 to read data from
1	[2]	Reserved	Must be 0
1	[1:0]	LUT Address	The 2 MSBs from LUT Address, 9:8
2	[6:0]	Chip Address	
3	[7:0]	LUT Address	The 8 LSBs of the LUT Address, 7:0
4	[7:0]	Data Byte 1 – Data [15:8]	Master sends out the SCLK pulses and data is received on the SDO line
5	[7:0]	Data Byte 2 – Data [7:0]	

LCL_LUT_WR Timing Sequence



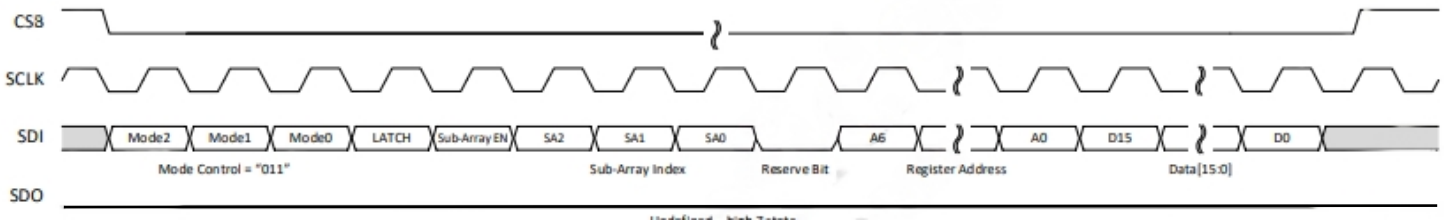
LCL_LUT_WR Command Bit Sequence

Byte 1								Byte 2								Byte 3								Byte 4	Byte 5
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7...0	7...0
MODE			LUT Channel		RES	LUT Address		RES	Chip Address							LUT Address								Data Read	
1	1	0	CH1	CH2	0	LA9	LA8	0	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0	LA7	LA6	LA5	LA4	LA3	LA2	LA1	LA0	D15...D8	D7...D0

LCL_LUT_RD Command Bit Description

Byte	Bit	Description	Comment
1	[7:5]	Mode Control	For Local LUT Read, mode = 110
1	[4:3]	Channel Select	Choose between CH0 – CH3 to read data from
1	[2]	Vn	0 = Reads from VLUT
1	[1:0]	LUT Address	The 2 MSBs from LUT Address, 9:8
2	[6:0]	Chip Address	
3	[7:0]	LUT Address	The 8 LSBs of the LUT Address, 7:0
4	[7:0]	Data Byte 1 – Data [15:8]	Data sent on the SDI is stored to the selected LUT
5	[7:0]	Data Byte 2 – Data [7:0]	

GBL_LUT_WR Timing Sequence



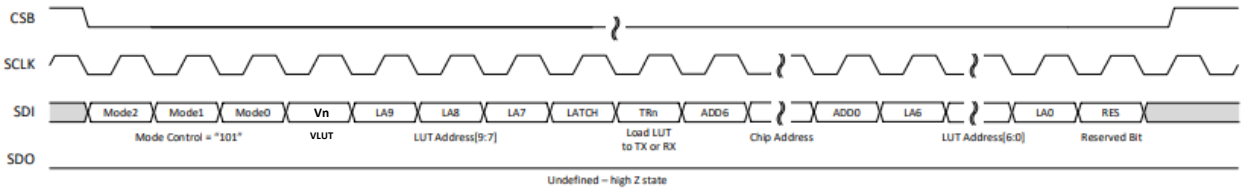
GBL_LUT_WR Command Bit Sequence

Byte 1								Byte 2								Byte 3								Byte 4
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	15... 8
Mode			LUT Channel		LUT SEL	LUT Address		LUT Address								Data								
0	1	0	Latch	SE	SA2	SA1	SA0	0	A6	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7... D0

GBL_LUT_WR Command Bit Description

Byte	Bit	Description	Comment
1	[7:5]	Mode Control	For Global LUT Write, mode 010
1	[4:3]	LUT Channel	Choose between CH0 – CH3 to read data from
1	[2]	Vn	0 = Reads from VLUT
1	[1:0]	LUT Address	The 2 MSBs from LUT Address, 9:8
2	[7:0]	LUT Address	The 8 LSBs of the LUT Address, 7:0
3	[7:0]	Data Byte 1 – Data [15:8]	Data sent on the SDI is stored to the selected LUT
4	[7:0]	Data Byte 2 – Data [7:0]	

LCL_FST_BM_STR Timing Sequence



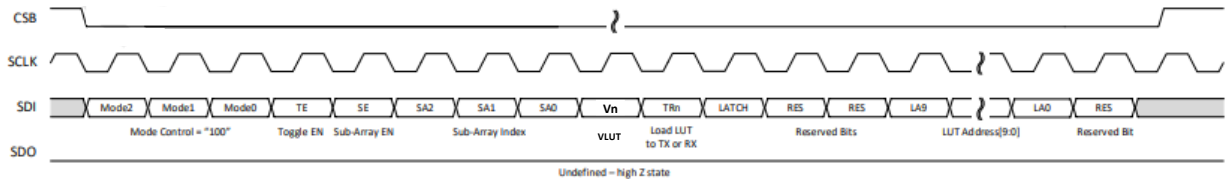
LCL_FST_BM_STR Command Bit Sequence

Byte 1								Byte 2								Byte 3							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Mode Control			LUT SEL	LUT Address			RF Load	TRX	Chip Address							LUT Address							
1	0	1	0	LA9	LA8	LA7	Latch	TRn	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0	LA6	LA5	LA4	LA3	LA2	LA1	LA0	RES

LCL_FST_BM_STR Command Bit Description

Byte	Bit	Description	Comment
1	[7:5]	Mode Control	For Local Fast Steering, mode = 101
1	[4]	Vn	0 = Load V-pol channels from VLUT
1	[3:1]	LUT Address	The 3 MSBs of the LUT Address, [9:7]
1	[0]	Latch	0 = Load the LUT Data onto only the buffers 1 = Load the LUT Data to the buffers and the SET Registers
2	[7]	TRn	0 = Loads LUT data to the RX channels. Also enables the RX channels 1 = Loads LUT data to the TX channels. Also enables the TX Channels.
2	[6:0]	Chip Address	
3	[7:1]	LUT Address	The 7 LSBs of the LUT Address, [6:0].

GBL_FST_BM_STR Timing Sequence



GBL_FST_BM_STR Command Bit Sequence

Byte 1								Byte 2								Byte 3							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Mode			Toggle	SE Enable	Sub-Array Idx			LUT SEL	TRX	RF Load	RES		LUT Address											
1	0	0	TE	SE	SA2	Latch	SA0	0	TRn	Latch	RES	RES	LA9	LA8	LA7	LA6	LA5	LA4	LA3	LA2	LA1	LA0	RES

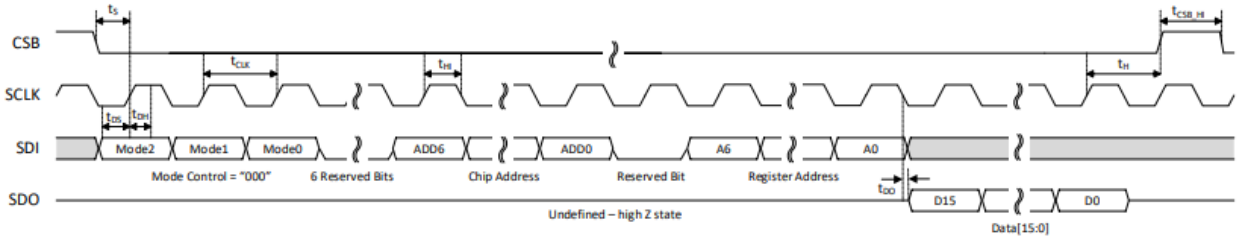
GBL_FST_BM_STR Command Bit Description

Byte	Bit	Description	Comment
1	[7:5]	Mode Control	For Global Fast Beam Steering, mode = 100
1	[4]	Toggle Enable (TE)	0 = No LUT Increment 1 = After Byte 3, every SCLK pulse increments the LUT address and loads the contents to the register
1	[3]	Sub-Array Enable (SE)	0 = Command executed on all chips 1 = Command executed on chips with matching sub-array
1	[2:0]	Sub-Array Index	If SE is set, data is written only when this index matches with the chip's sub-array index (Stored in register 0x0)
2	[7]	Vn	0 = Load V-pol channels from VLUT
2	[6]	TRn	0 = Loads LUT data to the RX channels. Also enables the RX channels 1 = Loads LUT data to the TX channels. Also enables the TX Channels.
2	[5]	Latch	0 = Load the LUT Data onto only the buffers 1 = Load the LUT Data to the buffers and the SET Registers
2	[2:0]	LUT Address	The 3 MSBs of the LUT Address, [9:7]
3	[7:1]	LUT Address	The 7 LSBs of the LUT Address, [6:0]

SPI Timing Typical Specifications

Symbol	Test Condition	Minimum	Typical	Maximum	Unit
T_S	CSB to SCLK setup time	2	-	-	Ns
T_{DS}	SDI data setup time	2	-	-	Ns
T_{DH}	SDI data hold time	4.2	-	-	Ns
T_{CLK}	SCLK period	10.5	-	-	Ns
T_{HI}	SCLK high time	5.25	-	-	Ns
T_{DO}	SCLK falling edge to valid SDO (first valid output in a READ operation)	5.1	-	-	Ns
T_H	SCLK to CSB hold time	7	-	-	Ns
T_{CSB_HI}	CSB high time	7	-	-	ns

Timing Specification Diagram



Control Configuration Register (CTRL_CFG)

Offset Address: 00h Default Value: 0000h

Bit	Field	Type	Description
15	IO_Test	WO	IO test mode for IO's VIL/VIH and MISO's VOL/VOH tests, only reset by power-on reset. In IO test mode, MISO pin is the output pin and its logic is RESET OR SPI_CSB OR SPI_CLK OR SPI_MOSI OR ADD0 OR ADD1 OR ADD2 OR ADD3 OR STROBE_IN
14	RSV	WO	Reserved.
13	SCAN_MODE	WO	Enable scan mode.
12	RESET	WO	1 = reset the chip – auto self-reset to 0
11	SHIFTREG_ADDR_EN	RO	1 = Shift register address is programmed and effective
10	SHIFTREG_ADDR_PROG	WO	8-bit shift register is placed between ADD0 pn (in) and ADD1 pin (out). To program the address, set this bit, then without releasing CSB, send in 8-bit data to ADD0 pin starting with LSB. Existing data is pushed out of ADD1 pin. New chip address = shift_reg[7:0]
9:7	SA_IDX	RW	Sub-Array Index
6:4	STROBE_PROG	RW	Program the strobe pin functionality. 000 = Latch buffers 001 = VTRX toggle 011 = H and V TRX toggle 100 = V LUT increment (enabled RX/TX) 110 = H and V LUT increment (enabled RX/TX)
2	V_TRn	RW	This bit is identical to VLUT[14]. Changing one will change the other. 0 = RXV enabled. 1 = TXV enabled.
0	V_EN	RW	Enable V channels

Vertical-Polarization LUT Address Pointer Register (VLUT)

Offset Address: 01h Default Value: 000Fh

Bit	Field	Type	Description
15	RSV	RO	Reserved
14	TRn	RW	This bit is identical to CTRL_CFG[2]. Changing one will change the other. 0= RXV enabled 1 = TXV enabled.
13:4	VLUT_PTR	RW	Updated when Global or Local FBS command is issued. When written to, channel SET register buffers are loaded with LUT data.
3	V4_EN	RW	Enable channel V4 when V_EN (CTRL_CFG[0]) = 1
2	V3_EN	RW	Enable channel V3 when V_EN (CTRL_CFG[0]) = 1
1	V2_EN	RW	Enable channel V2 when V_EN (CTRL_CFG[0]) = 1
0	V1_EN	RW	Enable channel V1 when V_EN (CTRL_CFG[0]) = 1

Master Bias Control Register 1 (MBIAS)

Offset Address: 05h Default Value: 8093h

Bit	Field	Type	Description
15:12	SCTAT_CTRL	RW	Super CTAT Bias control
11:9	SCTAT_TRIM	RW	Super CTAT Bias trim
8	SCTAT_EN	RW	Super CTAT Bias enable
7:5	PTAT2_SLOPE	RW	$PTAT^2$ slope control
4:2	PTADJ	RW	Internal reference current generator level control. ±30% reference current adjustment

PDET Enable Register (SENS_EN)

Offset Address: 06h Default Value: 0000h

Bit	Field	Type	Description
15:13	RSV	RW	Reserved
12:9	TSENS_SEL	RW	<1XXX> = TSENS_CORE enable <0111-0100> = H4-H1 <0011-0000> = V4-V1
8	TSENS_EN	RW	TSENSE Engine enable
7	RES	RW	Reserved
6	RES	RW	Reserved
5	RES	RW	Reserved
4	RES	RW	Reserved
3	VTX4_PDET_EN	RW	PDET V4 enable
2	VTX3_PDET_EN	RW	PDET V3 enable
1	VTX2_PDET_EN	RW	PDET V2 enable
0	VTX1_PDET_EN	RW	PDET V1 enable

Master Bias Control Register 2 (SENS_CTRL)

Offset Address: 07h Default Value: 0630h

Bit	Field	Type	Description
15:12	RSV	RW	Reserved
11:10	PD_BIAS_BUF_PROF	RW	PDET Buffer Bias profile
9:7	PD_BIAS_BUF_CTRL	RW	PDET Buffer Bias control
6:5	PD_BIAS_PROF	RW	PDET Bias profile
4:2	PD_BIAS_CTRL	RW	PDET Bias control
1	PD_BIAS_EN	RW	PDET Bias enable
0	TSENS_CHOPPER_EN	RW	TSENS Chopper enable

Chip ID Register (CHIP_ID)

Offset Address: 08h Default Value: 1300h

Bit	Field	Type	Description
15:14	ID_CLASS	RO	0 = Beamformer
13:12	ID_FREQ	RO	0 = 26 GHz 1 = 28 GHz 2 = 39 Ghz
11:8	BASE_REV	RO	Base Layer revision 1 = V1XY 2 = V2XY 3 = V3XY 4 = V4XY
7:4	METAL_REV	RO	Metal layer revision. X in V1XY
3:0	VARIANTS	RO	Variant number. Y in V1XY

SRAM BIST Register (BIST)

Offset Address: 09h Default Value: 0000h

Bit	Field	Type	Description
15:8	RSV	RO	Reserved
7	SRAM_DONE	RO	SRAM access (initialization, BIST, or CRC) status 0 = SRAM access is requested 1 = SRAM access is done
6:4	SRAM_ERR	RO	Number of SRAM error times during SRAM BIST. When the number exceeds 7, it will be kept at 7
3	SRAM_SEL	RW	0 = V-polarization SRAM
2	SRAM_CRC	RW	SRAM CRC check request Request SRAM CRC by writing 1 The SRAM CRC algorithm is as follows: 1. Initial value is 0xFFFF 2. CRC generator is $x^{16}+x^{12}+x^5+1$ 3. Sequence is: • N = 0 • Get data from LUT[N] • Do CRC on channel 1 data (bit11, bit10, …, bit1, bit 0 • Do CRC on channel 2, 3, and 4 • If N = 1023, finih CRC check; else do N = N+1 and go to step b
1	SRAM_BIST	RW	SRAM BIST request Request SRAM BIST by writing 1
0	SRAM_INIT	RW	SRAM initialization request (initialize all SRAM data to 0) Request SRAM initialization by writing 1

SRAM CRC Result Register (CRC_RESULT)

Offset Address: 0Ah Default Value: 0000h

Bit	Field	Type	Description
15:0	CRC_RESULT	RO	16-bit SRAM CRC result

ADC Channel Select Register 1 (ADC_SEL1)

Offset Address: 0Bh Default Value: 0000h

Bit	Field	Type	Description
15	EXT7	RW	Output data saved in register address 0x7F
14	EXT6	RW	Vbg_ptat
13	EXT5	RW	Vbg_por
12	EXT4	RW	DVDD/2
11	EXT3	RW	VDD/2
10	EXT2	RW	IDC_TEST set by ADD_CTRL: 50µA sent to AOUT pin
9	EXT1	RW	IDC_TEST set by ADD_CTRL: 50µA drawn on the internal 10kΩ resistor. Expected voltage = 0.5V
8	RES	RW	Reserved
7	RES	RW	Reserved
6	RES	RW	Reserved
5	RES	RW	Reserved
4	TSENSE_V4	RW	Output data saved in register address 0x74
3	TSENSE_V3	RW	Output data saved in register address 0x73
2	TSENSE_V2	RW	Output data saved in register address 0x72
1	TSENSE_V1	RW	Output data saved in register address 0x71
0	TSENSE_CORE	RW	Output data saved in register address 0x70

ADC Channel Select Register 1 (ADC_SEL1)

Offset Address: 0Ch Default Value: 0000h

Bit	Field	Type	Description
15	RES	RW	Reserved
14	RES	RW	Reserved
13	RES	RW	Reserved
12	RES	RW	Reserved
11	PDREF_V4	RW	Output data saved in register 0x6B
10	PDREF_V3	RW	Output data saved in register 0x6A
9	PDREF_V2	RW	Output data saved in register 0x69
8	PDREF_V1	RW	Output data saved in register 0x68
7	RES	RW	Reserved
6	RES	RW	Reserved
5	RES	RW	Reserved
4	RES	RW	Reserved
3	PD_V4	RW	Output data saved in register 0x63
2	PD_V3	RW	Output data saved in register 0x62
1	PD_V2	RW	Output data saved in register 0x61
0	PD_V1	RW	Output data saved in register 0x60

ADC Control Register (ADC_CONTROL)

Offset Address: 0Dh Default Value: 0000h

Bit	Field	Type	Description
15:14	RSV	RW	Reserved
13:11	IDC_TEST	RW	Tested on EXT1 000 = Disabled 001 = Ibg_50µA 010 = Ipt_50µA 011 = Ipt2_50µA 100 = Isct_50µA
10	PD_DIFF_MODE	RW	0 = Software diff (PD_V1 = PD-PDREF 1 = No diff
9:8	OSC_FREQ	RW	Oscillator frequency. 0 = 80 Mhz 1 = 40 MHz 2 = 20 Mhz 3 = OFF
7	OSC_EN	RW	Oscillator enable
6:5	AOUT_SEL	RW	AOUT mux selection. 0 = ADC input specified by registers ADC_SEL 1 and ADC_SEL2 1 = cbn1_test 2 = vref(v1p5) 3 = vcm(v0p9)
4	AOUT_EN	RW	AOUT mux enable
3	LSB_SEL	RW	Turn down LSB. 0 = LSB is VREF/1023 1 = LSB is Vref/1055
2	CHOPPER_EN	RW	Chopper enable
1	ADC_I_2X	RW	Double ADC bias current
0	ADC_START	RW	Start ADC operation

ADC Clock Control Register (ADC_CLK)

Offset Address: 0Eh Default Value: 0000h

Bit	Field	Type	Description
15	RSV	RW	Reserved
14:12	ADC_AVG	RW	0 = No averaging 1 - 6 = Averaging count = 2^{ADC_AVG} 7 = Averaging count 2^6
11:8	BASE_CLK_CTRL	RW	Select base clock (BASE_CLK) as OSC_60MHz/(N+1)
7:4	ADC_CLK_HIGH	RW	Select ADC clock's high width as BASE_CLK*(N+1)
3:0	ADC_CLK_LOW	RW	Select ADC clock's low width as BASE_CLK*(N+1)

OTP Control Register (OTP_CTRL)

Offset Address: 0Fh Default Value: 0000h

Bit	Field	Type	Description
15:13	RSV	RO	Reserved
12:10	OTP_WR_BIT	RW	Bit number to burn during program mode
9:6	OTP_RW_ADDRESS	RW	OTP Read/Write address back selection
5	OTP_PROG	RW	OTP program mode
4	OTP_POR	RW	OTP POR
3:2	OTP_CUR	RW	OTP current control
1	OTP_READ	RW	OTP Read enable
0	OTP_EN	RW	OTP enable

PCM Control Register (PCM_CTRL)

Offset Address: 10h Default Value: 0000h

Bit	Field	Type	Description
15:7	RSV	RO	Reserved
6:3	PCM_CLK_DIV	RW	Counter duration = Tspi_clk/(PCM_CLK_DIV+1)
2:1	PCM_CH_SEL	RW	PCM channel selection 0 = BJT ring oscillator 1 = R ring oscillator 2 = RC ring oscillator
0	PCM_START	RW	PCM start (auto-reset)

TOP Spare Register 1 (SPARE1)

Offset Address: 11h Default Value: 0000h

Bit	Field	Type	Description
15:0	RSV	RW	Reserved

TOP Spare Register 2 (SPARE2)

Offset Address: 12h Default Value: 0000h

Bit	Field	Type	Description
15:0	RSV	RW	Reserved

PCM Data Register 1 (DATA_PCM1)

Offset Address: 15h Default Value: 0000h

Bit	Field	Type	Description
15:12	RSV	RO	Reserved
11:0	DATA_CH1	RO	CH1: BJT

PCM Data Register 2 (DATA_PCM1)

Offset Address: 16h Default Value: 0000h

Bit	Field	Type	Description
15:12	RSV	RO	Reserved
11:0	DATA_CH2	RO	CH2: R

PCM Data Register 3 (DATA_PCM1)

Offset Address: 17h Default Value: 0000h

Bit	Field	Type	Description
15:12	RSV	RO	Reserved
11:0	DATA_CH3	RO	CH3: RC

TP Data Register 1 (DATA_OTP1)

Offset Address: 18h Default Value: 0000h

Bit	Field	Type	Description
15:8	DATA_OTP_REG1	RO	OTP address = 4'd1
7:0	DATA_OTP_REG0	RO	OTP address = 4'd0

OTP Data Register 2 (DATA_OTP1)

Offset Address: 19h Default Value: 0000h

Bit	Field	Type	Description
15:8	DATA_OTP_REG3	RO	OTP address = 4'd3
7:0	DATA_OTP_REG2	RO	OTP address = 4'd2

OTP Data Register 3 (DATA_OTP1)

Offset Address: 1Ah Default Value: 0000h

Bit	Field	Type	Description
15:8	DATA_OTP_REG5	RO	OTP address = 4'd5
7:0	DATA_OTP_REG4	RO	OTP address = 4'd4

OTP Data Register 4 (DATA_OTP1)

Offset Address: 1Bh Default Value: 0000h

Bit	Field	Type	Description
15:8	DATA_OTP_REG7	RO	OTP address = 4'd7
7:0	DATA_OTP_REG6	RO	OTP address = 4'd6

OTP Data Register 5 (DATA_OTP1)

Offset Address: 1Ch Default Value: 0000h

Bit	Field	Type	Description
15:8	DATA_OTP_REG9	RO	OTP address = 4'd9
7:0	DATA_OTP_REG8	RO	OTP address = 4'd8

OTP Data Register 6 (DATA_OTP1)

Offset Address: 1Dh Default Value: 0000h

Bit	Field	Type	Description
15:8	DATA_OTP_REG11	RO	OTP address = 4'd11
7:0	DATA_OTP_REG10	RO	OTP address = 4'd10

OTP Data Register 7 (DATA_OTP1)

Offset Address: 1Eh Default Value: 0000h

Bit	Field	Type	Description
15:8	DATA_OTP_REG13	RO	OTP address = 4'd13
7:0	DATA_OTP_REG12	RO	OTP address = 4'd12

OTP Data Register 8 (DATA_OTP1)

Offset Address: 1Fh Default Value: 0000h

Bit	Field	Type	Description
15:8	DATA_OTP_REG15	RO	OTP address = 4'd15
7:0	DATA_OTP_REG14	RO	OTP address = 4'd14

Vertical TRX Block Enable Register (ENV)

Offset Address: 20h Default Value: 1F0Fh

Bit	Field	Type	Description
15:13	RSV	RW	Reserved
12	TX_PA_EN	RW	TX PA enable
11	TX_DA_EN	RW	TX DA enable
10	TX_PS_EN	RW	TX phase shifter enable
9	TX_VGA2_EN	RW	TX VGA2 enable
8	TX_VGA1_EN	RW	TX VGA1 enable
7:4	RSV	RW	Reserved
3	RX_LNA1_EN	RW	RX LNA1 enable
2	RX_LNA2_EN	RW	RX LNA2 enable
1	RX_PS_EN	RW	RX phase shifter enable
0	RX_VGA_EN	RW	RX VGA enable

Vertical LNA Control Register (RXV_LNA)

Offset Address: 21h Default Value: 0BA8h

Bit	Field	Type	Description
15:12	RSV	RW	Reserved
11	RX_LNA2_PT	RW	0 = PTAT current source 1 = $PTAT^2$ current source
10:8	RX_LNA2_BIAS	RW	Set LNA2 bias
7	RX_LNA1_PT	RW	0 = PTAT current source 1 = $PTAT^2$ current source
6:3	RX_LNA1_BIAS	RW	Set LNA1 bias
2:1	RX_LinMode	RW	0 = Max gain 1 = LNA1 gain reduced by 3dB 2 = LNA2 gain reduced by 3dB 3 = Both LNA1 and LNA2 gain reduced (6dB total)
0	RX_LinMODE_ExtPinEN	RW	0 = LNA linearity mode as defined by RX_LinMode 1 = LNA linearity mode gated by LNASW pin

Setting	LNA1 Attenuation	LNA2 Attenuation
0	0dB	0dB
1	3dB	0dB
2	0dB	3dB
3	3dB	3dB

RX_LinMode_Ext PinEN	LNASW Pin	Linearity Mode
0	0	1 (RX_LinMode)
0	1	1 (RX_LinMode)
1	0	1 (RX_LinMode)
1	1	0 (Max Gain)

Vertical RX PS/VGA Control Register (RXV_PS_VGA)

Offset Address: 22h Default Value: 020Ch

Bit	Field	Type	Description
15:11	RSV	RW	Reserve
10	RX_VGA_PT	RW	0 = PTAT current source 1 = $PTAT^2$ current source
9:7	RX_VGA_BIAS	RW	Set VGA bias
6:4	RX_PS_CORR	RW	Phase shifter correction
3	RX_PS_PT	RW	0 = PTAT current source 1 = $PTAT^2$ current source
2:0	RX_PS_BIAS	RW	Set phase shifter bias

Vertical RX Spare Register 1 (RXV_SPARE1)

Offset Address: 23h Default Value: 0000h

Bit	Field	Type	Description
15:0	RSV	RW	Reserved

Vertical RX Spare Register 2 (RXV_SPARE2)

Offset Address: 24h Default Value: 0000h

Bit	Field	Type	Description
15:0	RSV	RW	Reserved

Vertical TX PA Control Register (TXV_PA)

Offset Address: 25h Default Value: 1CB7h

Bit	Field	Type	Description
15:13	RSV	RW	Reserved
12	TX_PA_FB	RW	PA RC feedback control
11:10	TX_PA_BIASR	RW	PA bias resistor tuning
9:8	TX_PA_CASCCAP	RW	PA cascade capacitor tuning
7	TX_PA_BG	RW	0 = PTAT current source 1 = Band-gap current source
6:4	TX_PA_CASCBIAS	RW	PA cascade bas
3:0	TX_PA_BIAS	RW	PA core bias

Vertical TX PA Control Register (TXV_PA)

Offset Address: 26h Default Value: 00E9h

Bit	Field	Type	Description
15:13	RSV	RW	Reserved
12	TX_DA_INPUTRTUNE	RW	Driver input resitor
11:10	TX_DA_INTERCTUNE	RW	0 = PTAT current source 1 = $PTAT^2$ current source
9:8	TX_DA_INPUTCTUNE	RW	Set phase shifter bias
7	TX_DA_PT	RW	0 = PTAT current source 1 = $PTAT^2$ current source
6:4	TX_DA_CASCBIAS	RW	Set VGA2 bias
3:0	TX_DA_BIAS	RW	0 = PTAT current source 1 = $PTAT^2$ current source

Vertical TX PS/VGA Control Register (TXV_DRV)

Offset Address: 27h Default Value: 0C5Ch

Bit	Field	Type	Description
15	RSV	RW	Reserved
14:12	TX_PS_CORR	RW	Phase shifter correction
11	TX_PS_PT	RW	0 = PTAT current source 1 = $PTAT^2$ current source
10:8	TX_PS_BIAS	RW	Set phase shifter bias
7	TX_VGA2_PT	RW	0 = PTAT current source 1 = $PTAT^2$ current source
6:4	TX_VGA2_BIAS	RW	Set VGA2 bias
3	TX_VGA1_PT	RW	0 = PTAT current source 1 = $PTAT^2$ current source
2:0	TX_VGA1_BIAS	RW	Set VGA1 bias

Vertical TX Spare Register 1 (TXV_SPARE1)

Offset Address: 28h Default Value: 0000h

Bit	Field	Type	Description
15:0	RSV	RW	Reserved

Vertical TX Spare Register 2 (TXV_SPARE2)

Offset Address: 29h Default Value: 0000h

Bit	Field	Type	Description
15:0	RSV	RW	Reserved

Vertical PDET Control Register (PDETV)

Offset Address: 2Ah Default Value: 0042h

Bit	Field	Type	Description
15:8	RSV	RW	Reserved
7:5	PDET_ATEST	RW	PDET Atest control
4:3	PDET_Range	RW	Power range
2	PDET_AMPEN	RW	PDET differential amplifier enable
1:0	SW_BIAS	RW	RX antenna switch bias

Vertical RX SET Register (RXVn_SET) (n = 1 to 4)

Offset Address: 40h + 4*(n-1) Default Value: 40FFh

Bit	Field	Type	Description
15:8	RX_PHASE_CTRL	RW	RX phase control
7:0	RX_GAIN_CTRL	RW	RX gain control

Vertical TX SET Register (TXVn_SET) (n = 1 to 4)

Offset Address: 41h + 4*(n-1) Default Value: 00FFh

Bit	Field	Type	Description
15:8	TX_PHASE_CTRL	RW	TX phase control
7:0	TX_GAIN_CTRL	RW	TX gain control

Vertical RX Bias Register (RXVn_BIAS) (n = 1 to 4)

Offset Address: 42h + 4*(n-1) Default Value: 0003h

Bit	Field	Type	Description
15:4	SPARE	RW	SPARE
3	RX_GAIN_CTRL	RW	RX gain mode
2:0	RX_CH_BIAS	RW	RX channel bias

Vertical TX Bias Register (TXVn_BIAS) (n = 1 to 4)

Offset Address: 43h + 4*(n-1) **Default Value: 000Ch**

Bit	Field	Type	Description
15:4	RSV	RW	Reserved
3	TX_GAIN_CTRL	RW	TX gain mode
2:0	TX_CH_BIAS	RW	TX channel bias

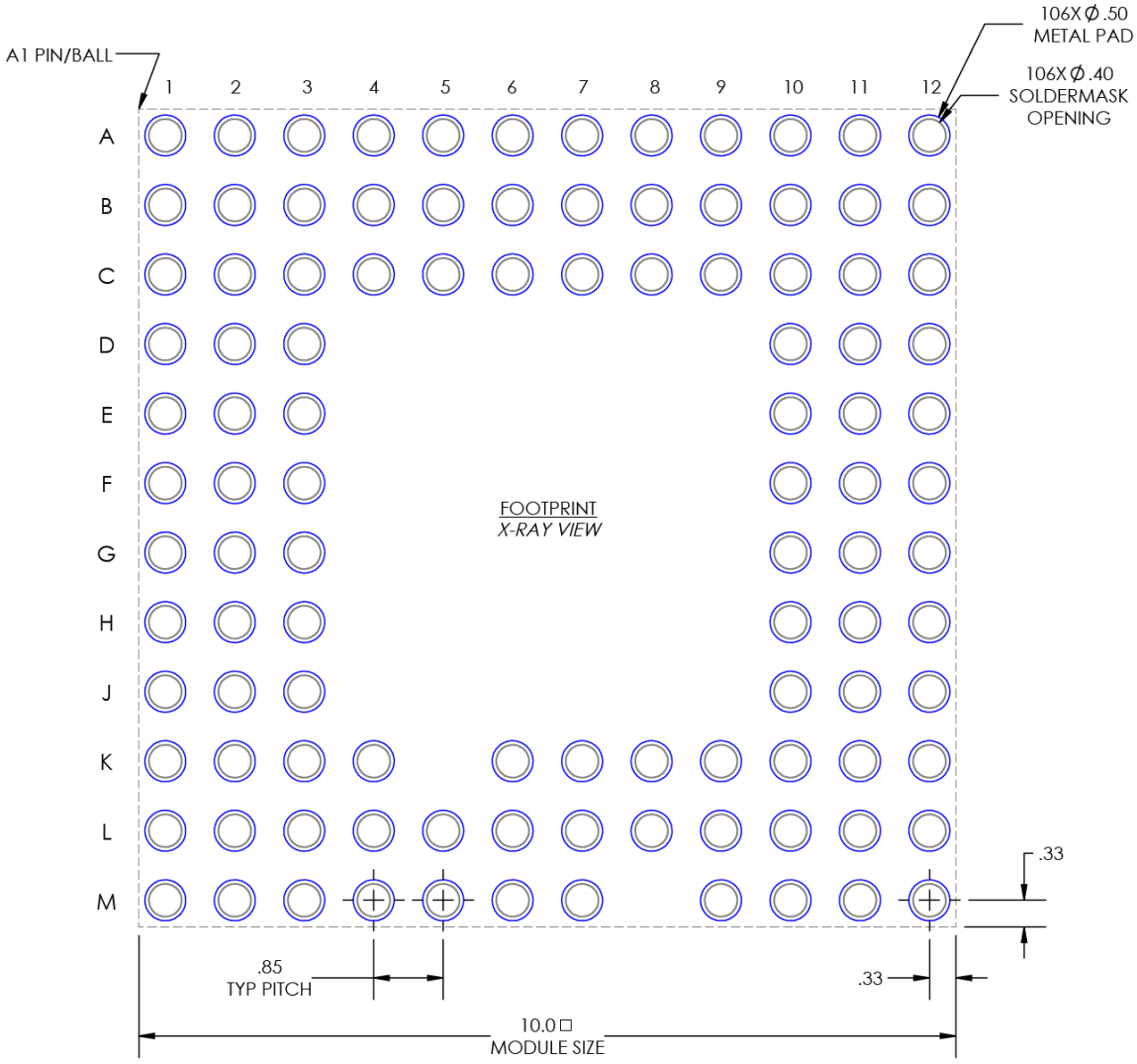
ADC DATA Register (DATA_ADC_CHn) (n = 1 to 32)

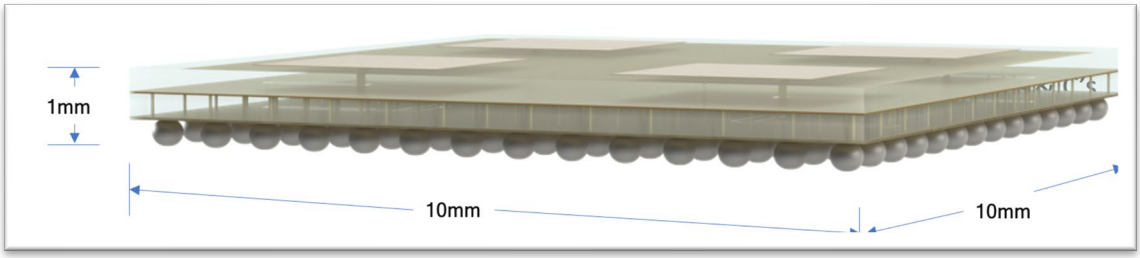
Offset Address: 60h + (n-1) **Default Value: 0000h**

Bit	Field	Type	Description
15:11	RSV	RO	Reserved
10	DONE	RO	ADC status
9:0	VALUE	RO	ADC data

Mechanical Footprint

Footprint





Ordering Guide

Model	Package Description
ED2-0023	Module in gel-pak
ED2-0023-TNR	Module in tape-and-reel packaging
ED2-0023-KIT	Module EVAL KIT (includes Module)
ED2-0023-000501	Eval Board without the Digital Board
ED2-0027	Digital board only