F84010

1.8GHz to 2.2GHz TX Frontend Module for 4G/5G Applications

The F84010 is a 1.8GHz to 2.2GHz multi-chip transmitter (TX) frontend module. The device is housed in an SMT package with RF input and output matched to 50Ω. The highly integrated single-channel module is designed to achieve up to 16W average output power (10dB output back-off) with high efficiency and gain.

Competitive Advantage

- Wide frequency coverage from 1.8GHz to 2.2GHz
- High average power efficiency
- FDD DPD friendly

Features

- Highly integrated single-channel TX frontend
  - Suitable for 5G FDD mMIMO systems
  - 1.8GHz to 2.2GHz (Bands n1, n2, n3, n25, and n66)
- Specifications at 16W average output power:
  - 46.5dB typical gain
  - > 47% PAE
  - < -30dBc Raw ACPR
  - 365MHz iBW
- RF input and output matched to 50Ω
- -40°C to 125°C operable temperature range
- 20 × 18 mm 22-LGA package

Applications

- Wireless infrastructure
- 5G active antenna systems
- General RF

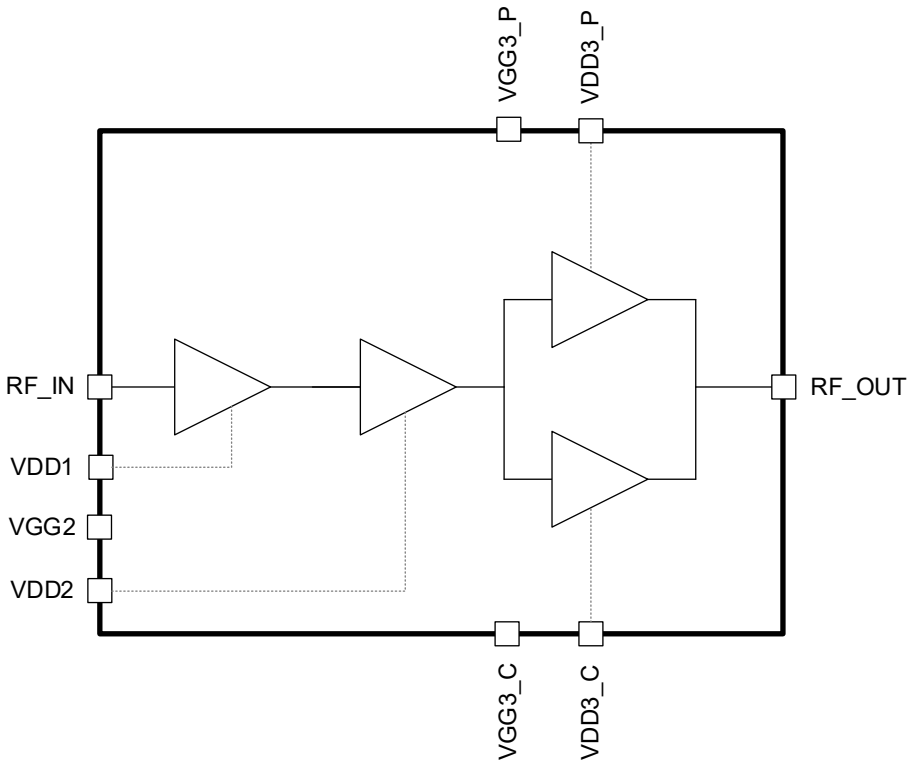


Figure 1. Block Diagram

Contents

Figures

Tables

1. Pin Information

1.1 Pin Assignments

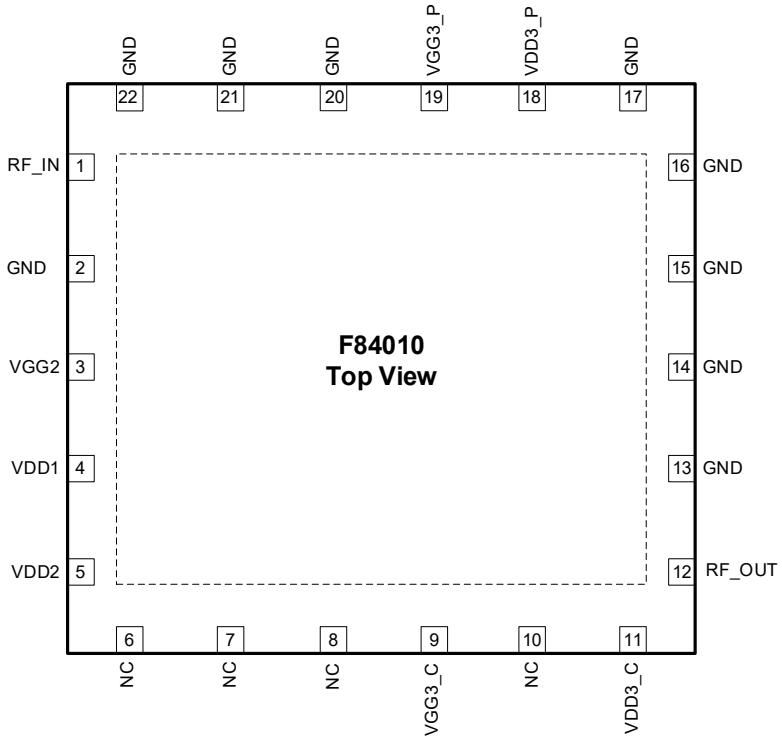


Figure 2. Pin Assignments – Top View

1.2 Pin Descriptions

Pin Number	Pin Name	Description
1	RF_IN	RF input. Matched to 50Ω. DC Blocked.
2, 13, 14, 15, 16, 17, 20, 21, 22	GND	Ground connection. Use a via as close to the pin as possible.
3	VGG2	This pin sets the gate voltage of the driver amplifier.
4	VDD1	Power supply pin for pre-driver. Use bypass capacitors as close to the pin as possible.
5	VDD2	Power supply pin for driver amplifier. Use bypass capacitors as close to the pin as possible.
6, 7, 8, 10	NC	No connection. These pins can be left unconnected.
9	VGG3_C	This pin sets the gate voltage of the final stage carrier amplifier.
11	VDD3_C	Power supply pin for the final stage carrier amplifier. Use bypass capacitors as close to the pin as possible.
12	RF_OUT	RF output. Matched to 50Ω. DC Blocked.
18	VDD3_P	Power supply pin for the final stage peaking amplifier. Use bypass capacitors as close to the pin as possible.
19	VGG3_P	This pin sets the gate voltage of the final stage peaking amplifier.

2. Specifications

2.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
VDD3_C to GND	-	55	V
VDD3_P to GND	-	55	V
VDD2 to GND	-	55	V
VDD1 to GND	-	8	V
VGG2 to GND	-10	0	V
VGG3_P to GND	-10	0	V
VGG3_C to GND	-10	0	V
Drain--Source Voltage VDS(max) [VGG = -10V, T_{case} = 25°C]	-	200	V
Exposed Pad Operating Temperature Range	-	125	°C
GaN Junction Temperature (T_{jmax_GaN})	-	250	°C
Storage Temperature Range (T_{stg})	-55	125	°C
Peak Input Power Pulsed CW, 250µs (on), 5% Duty Cycle, 1.8-2.2GHz	-	18	dBm
ESD Rating – Human Body Model (Tested per JS-001-2017)	-	1000	V
ESD Rating – Charged Device Model (Tested per JS-002-2018)	-	500	V
Moisture Sensitivity Rating (Per J-STD-020)	MSL3		-

2.2 Recommended Operating Conditions

Parameter	Condition	Minimum	Typical	Maximum	Unit
VDD3_C	-	-	48	50	V
VDD3_P	-	-	48	50	V
VDD2	-	-	48	50	V
VDD1	-	4.75	5	5.25	V
VGG2	-	-5	-2.7	-2.5	V
VGG3_P	-	-7	-6.5	-2.5	V
VGG3_C	-	-5	-2.7	-2.5	V
RF Frequency Range	-	1800	-	2200	MHz
Port Impedance	-	-	50	-	Ω
GaN Junction Temperature	-	-	-	225	°C

2.3 Thermal Specifications

Parameter	Symbol	Value	Unit
Active Die Surface to Case Thermal Resistance Infrared Measurement, evaluated at 85°C ambient	$\Theta_{SC\text{-}BOT}$	2.04	°C/W

2.4 Electrical Specifications – DC

Specifications apply at T_{EP} = 25°C unless otherwise stated.

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Driver, GaN + Final Stage Carrier and Peaking Stage, GaN – Off Characteristic						
Off-State Drain Leakage	ID(BR)	VDD2 = VDD3_P = VDD3_C = 150V VGG2 = VGG3_P = VGG3_C = -10V	-	0.01	1	mA/ mmdc
Off-State Gate Leakage	IGLK	VDD2 = VDD3_P = VDD3_C = 50V VGG2 = VGG3_P = VGG3_C = -5V	-	0.002	0.025	mA/ mmdc
Pre-driver, GaAs – On Characteristics						
Quiescent Current	ICQ	VDD1 = 5V	-	105	-	mA
Driver, GaN – On Characteristics						
Gate Threshold Voltage [1]	VGS(th)	VDD2 = 15V, ID = 0.1mA/mm	-	-3.0 ±0.5	-	Vdc
Gate Quiescent Voltage	VGS(q)	VDD2 = 48V, IDQ = 20mA	-	-2.7	-	Vdc
Final Carrier, GaN – On Characteristics						
Gate Threshold Voltage [1]	VGS(th)	VDD3_C = 15V, ID = 0.1mA/mm	-	-3.0 ±0.5	-	Vdc
Gate Quiescent Voltage	VGS(q)	VDD3_C = 48V, IDQ = 100mA	-	-2.7	-	Vdc
Final Peaking, GaN – On Characteristics						
Gate Threshold Voltage [1]	VGS(th)	VDD3_P = 15V, ID = 0.1mA/mm	-	-3.0 ±0.5	-	Vdc
Gate Quiescent Voltage	VGS(q)	VDD3_P = 48V, IDQ = 100mA	-	-6.5	-	Vdc

1. Driver and Final carrier side and peaking side are tied together for these measurements.

2.5 Electrical Specifications – RF

See the F84010 Typical Application Circuit. Specifications apply when operated as a power amplifier with VDD3_C = VDD3_P = VDD2 = 48V, VDD1 = 5V, IDQ_{VDD1} = 105mA, IDQ_{VDD2} = 20mA, VGG3_P = -6.5V, IDQ_{VDD3_C} = 100mA, Pavg = 16W, T_{EP} = 25°C, Z_S = Z_L = 50Ω. CW tests consist of a pulsed single tone at 10% duty cycle. LTE tests consist of a 1C 20MHz LTE signal with 10dB PAR at 0.01% probability on CCDF. Evaluation Kit trace and connector losses are de-embedded.

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Unit
VBW Resonance Point	VBWres	2-tone, 1MHz Tone Spacing (IMD Third Order Modulation Inflection Point)	-	600	-	MHz
Gain at Pavg	G	Pulsed CW, 10% duty cycle f_{RF} = 1800MHz, T_{EP} = 25°C	-	46.5	-	dB
		Pulsed CW, 10% duty cycle f_{RF} = 2000MHz, T_{EP} = 25°C	-	46.5	-	
		Pulsed CW, 10% duty cycle f_{RF} = 2200MHz, T_{EP} = 25°C	-	46.5	-	
Gain Flatness	G_{FLAT}	Within any 400MHz BW	-	1.5	-	dB
Raw ACPR at Pavg	ACP_{RAW1}	LTE 20MHz, 10dB PAR, T_{EP} = 25°C f_{RF} = 2000MHz, Pout = 42dBm	-	-30	-	dBc
Module Efficiency at Pavg	EFF	LTE 20MHz, 10dB PAR, T_{EP} = 25°C f_{RF} = 2000MHz, Pout = 42dBm	-	47	-	%
Pout at 3dB Compression Point	P3dB	Pulsed CW, 10% duty cycle f_{RF} = 1800MHz, T_{EP} = 25°C	-	51.5	-	dBm
		Pulsed CW, 10% duty cycle f_{RF} = 2000MHz, T_{EP} = 25°C	-	51.5	-	
		Pulsed CW, 10% duty cycle f_{RF} = 2200MHz, T_{EP} = 25°C	-	51.5	-	
AM/PM at 3dB Compression Point	AMPM_3dB		-	-20	-	°
Gain Variation at Average Power over Temperature	ΔG_{TEMP}	Pulsed CW, 10% duty cycle f_{RF} = 2000MHz, T_{EP} = -40°C to 105°C	-	0.055	-	dB/°C
P3dB Variation over Temperature	$\Delta P3dB_{TEMP}$	Pulsed CW, 10% duty cycle f_{RF} = 2000MHz, T_{EP} = -40°C to 105°C	-	0.007	-	dB/°C

1. Items in the Minimum/Maximum columns in ***bold italics*** are confirmed by test with 1-tone CW signal. Items in the Minimum/Maximum columns NOT in bold italics are confirmed by design characterization.

3. Functional Information

3.1 Biasing Sequence

Bias ON the device:

1. Turn on +5V to the GaAs-HBT pre-driver drain (VDD1). Check pre-driver Idq~ 105mA
2. Turn on -6.5V to the gate of GaN driver (VGG2) and final-stage carrier and peak devices (VGG3_C and VGG3_P)
3. Turn on +48V to the drain GaN driver (VDD2) and final-stage carrier and peak devices (VDD3_C and VDD3_P)
4. Adjust VGG2 to get driver Idq~ 20mA (VGG2 ≈ −2.68V)
5. Adjust VGG3_C to get carrier device Idq~ 100mA (VGG3_C ≈ −2.73V)
6. Turn on RF input power.

Bias OFF the device:

1. Turn off RF input power.
2. Turn off the drain bias of the GaN driver (VDD2) and final-stage carrier and peak devices (VDD3_C and VDD3_P).
3. Turn off the gate bias of driver (VGG2) and final-stage carrier and peak (VGG3_C and VGG3_P).
4. Turn off the 5V drain bias of the GaAs-HBT Pre-Driver (VDD1).

4. Evaluation Board (EVB) Information

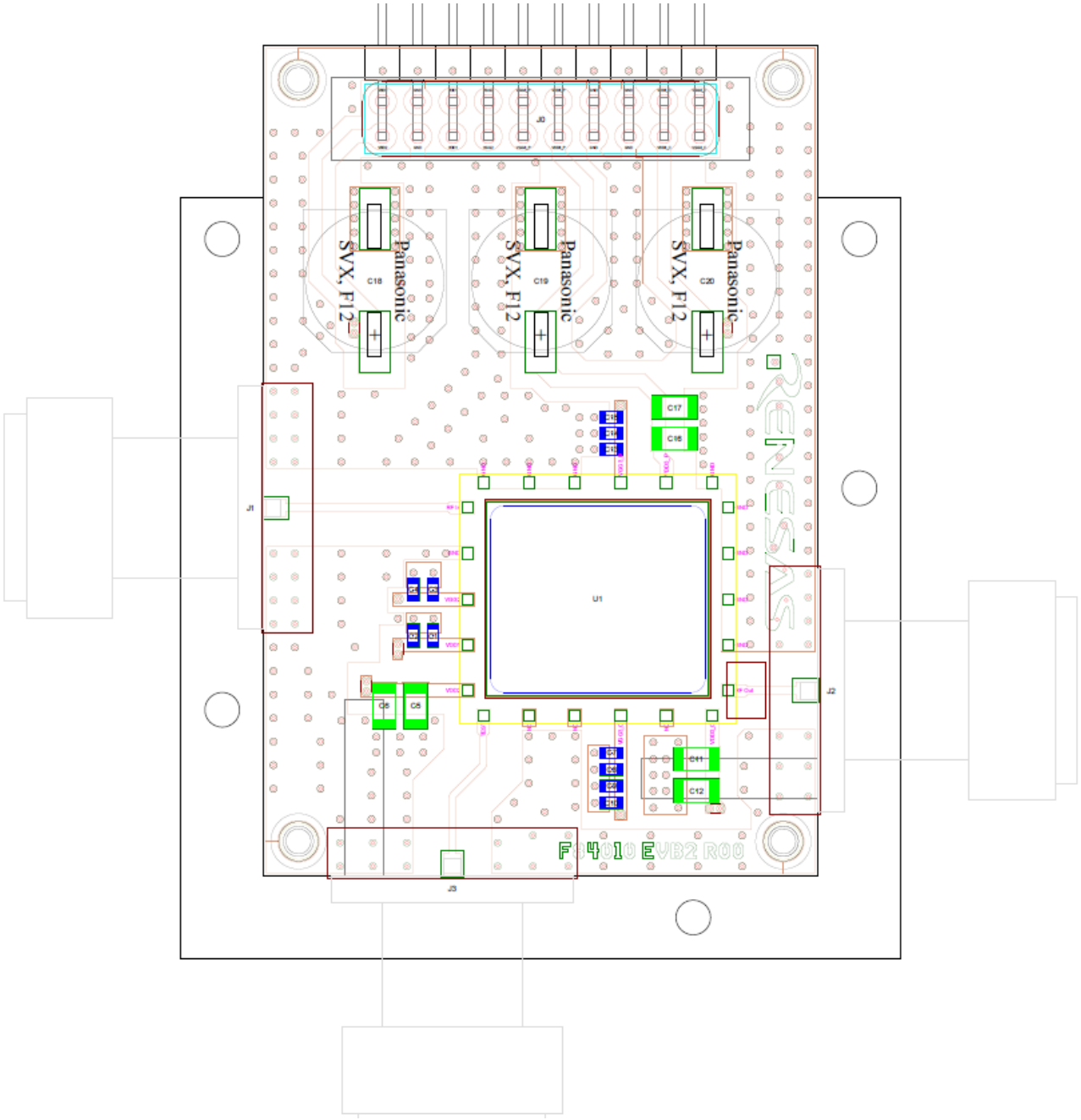


Figure 3. Evaluation Board – Front

4.1 Evaluation Board Schematic

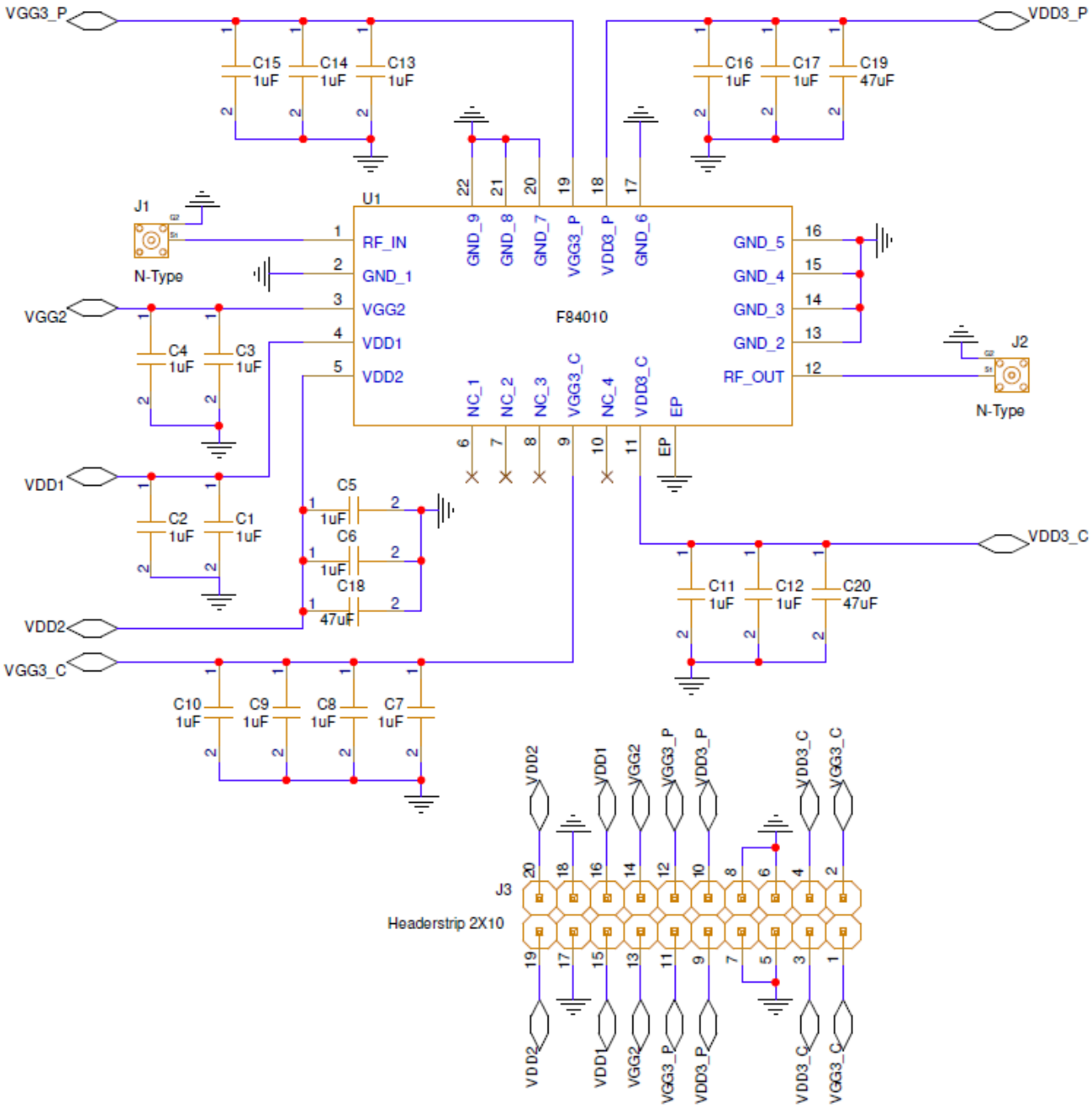


Figure 4. Evaluation Board Circuit Schematic

4.2 Bill of Materials

Table 1. Evaluation Board Bill of Materials (BOM)

Part Reference	Qty	Description	Part Number	Manufacturer
C1, C2, C3, C4, C7, C8, C9, C10, C13, C14, C15	11	1.0µF ± 10%, 25V, X7R Surface Mount Capacitor (0603)	GRT188R71E105KE13D	Murata Electronics
C5, C6, C11, C12, C16, C17	6	1.0µF ± 10%, 100V, X8L Surface Mount Capacitor (1206)	GCJ31CL8EL105KA07L	Murata Electronics
C18, C19, C20	3	47µF ± 20%, 100V Surface Mount Capacitor (F12)	APZ1012470M100R	Kyocera AVX
J3	1	Header, 2 Rows x 10 Columns (20 positions), 0.100" (2.54mm) Pitch, Right-Angle	HTSW-110-08-F-D-RA	Samtec
J1, J2	2	SMA Type N connector	ANO 5112-3340	Anoison
U1	1	Power Amplifier Module	F84010	Axiro

5. Package Outline Drawings

The package outline drawings are located at the end of this document. The package information is the most current data available and is subject to change without revision of this document.

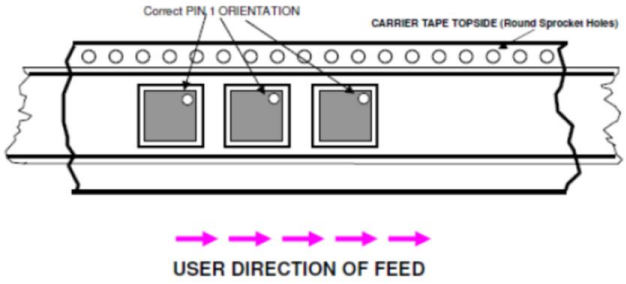
6. Marking Diagram

- Line 1: company name
- Line 2: truncated part number
- Line 3:
  - “$$” denotes the assembly site mark code
  - “YYMMDD” denotes the last two digits of the year, two digits of the month, and two digits of the day the part was assembled
  - “***” denotes the three-digit lot sequential code

7. Ordering Information

Part Number	Package Description	Carrier Type	Temperature Range
RRF84010-K00	20 × 18 mm 22-LGA	Tape and Reel (see Table 2)	-40°C to +125°C
RRF84010-B00	20 × 18 mm 22-LGA	Tray	-40°C to +125°C
RTKRF84010-2P0	Evaluation Board		

Table 2. Pin 1 Orientation in Tape and Reel Packaging

Part Number Suffix	Pin 1 Orientation	Illustration
K00	Quadrant 2 (EIA-481-D/E)	

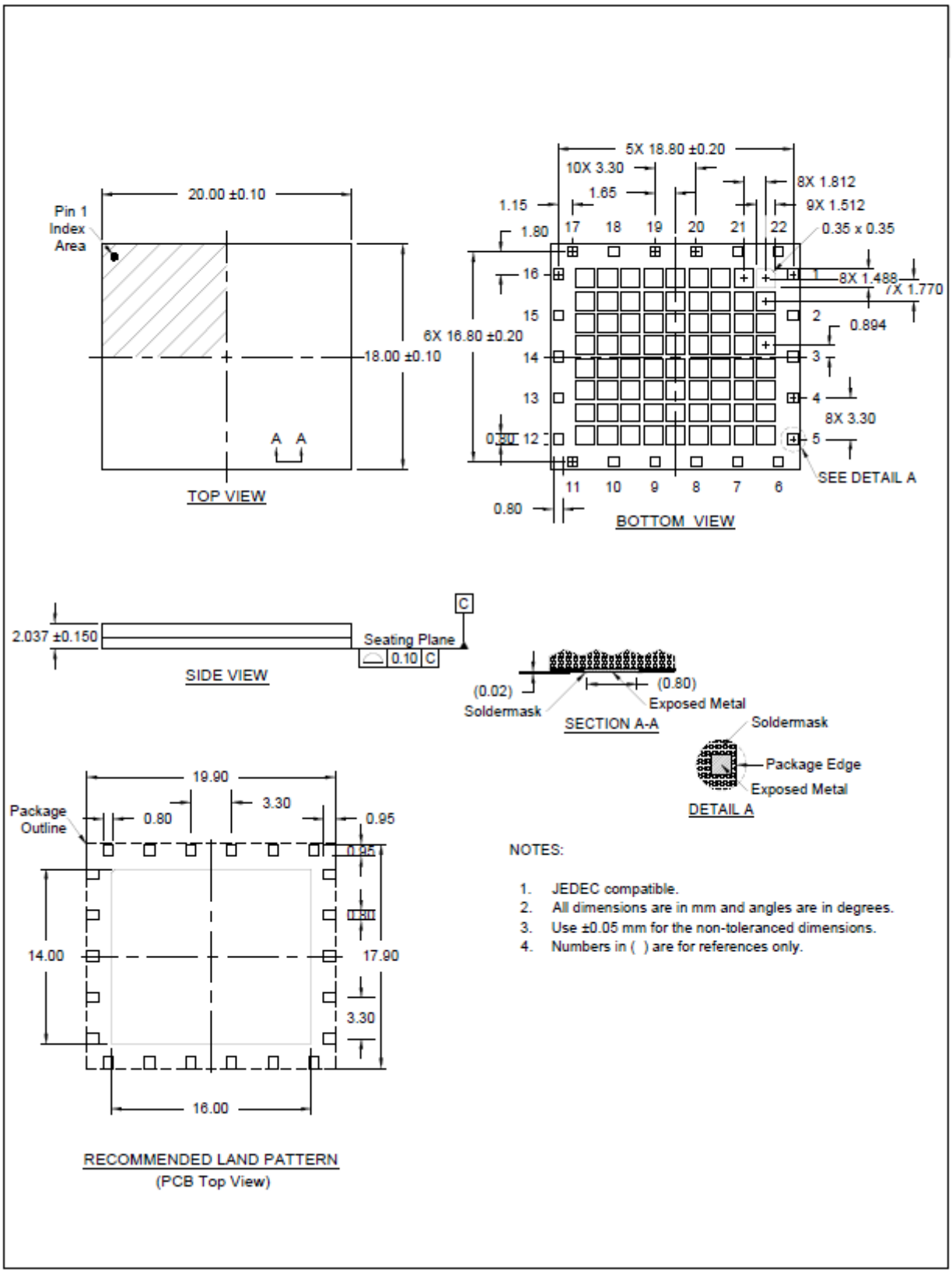
8. Revision History

Revision	Date	Description
0.13	Jun 3, 2025	▪ Updated branding
0.12	Nov 14, 2024	▪ Updated OPN
0.11	Oct 14, 2024	▪ Updated: Peak Input Power, POD, PAE, Schematic and BOM
0.10	Sep 16, 2024	▪ Updated RF Performance ▪ Updated Marking Diagram
0.09	Jul 9, 2024	▪ Updated EVB Schematic and BOM ▪ Updated Recommended Operating Maximum voltages ▪ Updated DC Electrical Specifications Off-State Drain Leakage test condition
0.08	Apr 29, 2024	▪ Updated BOM. ▪ Updated section 2.3 thermal specifications. ▪ Simplified section 2.1 ▪ Updated Biasing Sequence
0.07	Mar 19, 2024	▪ Updated section 2.3 thermal specifications. ▪ Updated Driver IDDQ.
0.06	Feb 7, 2024	▪ Updated pin 1 and pin 12 descriptions in section 1.2. ▪ Removed footnote 1 in section 2.1. ▪ Clarified language and updated Pre-Driver ICQ and GaN VGS values in section 2.4. ▪ Clarified header and test conditions in section 2.5. LTE test set reduced. Added Gain and P3dB over temperature value. Changed over temperature condition to +105°C. ▪ Removed empty sections.
0.05	Feb 6, 2024	▪ Updated first page, performance specifications. ▪ Updated package outline drawing (POD). ▪ Updated Biasing Sequence section.
0.04	Jan 8, 2024	Updated Thermal Specifications and package outline drawing.
0.03	Dec 11, 2023	Updated EVK information.
0.02	Dec 7, 2023	Updated Specifications. Completed other minor changes.
0.01	Aug 4, 2023	Initial release.

axiro
Engineering The Future

Package Outline Drawing

Package Code: SL0022AA
22-SIP LGA 20.0 x 18.0 x 2.04 mm Body, 3.3mm Pitch
PSC-5097-01, Revision: 00, Date Created: July 2, 2024



NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.