F6121

16-Channel Dual-Beam Rx Active Beamforming IC 10.7 to 12.75 GHz

The F6121 is a dual-beam receive active beamforming RFIC designed for application in Ku-Band SATCOM planar phased array antennas. The IC has eight RF input ports, two RF output ports, and 16 (8 per beam) phase/amplitude control channels. The eight input ports of the device can be driven by eight single-polarized elements, or four dual-polarized antenna elements.

Each channel has 6 bits of digital phase and gain control resolution spanning 360° and 28.4dB, enabling precise amplitude and phase adjustment for beam pattern and polarization control. The typical RMS phase and gain errors are 1.5° and 0.17dB, respectively.

The typical power consumption with nominal bias is 467mW or 29.2mW/ch in dual-beam mode and 276mW or 34.5mW/ch in single-beam mode. The typical electronic gain and noise figure are 10.7dB and 6.1dB, respectively, with 37dB of channel-to-channel isolation.

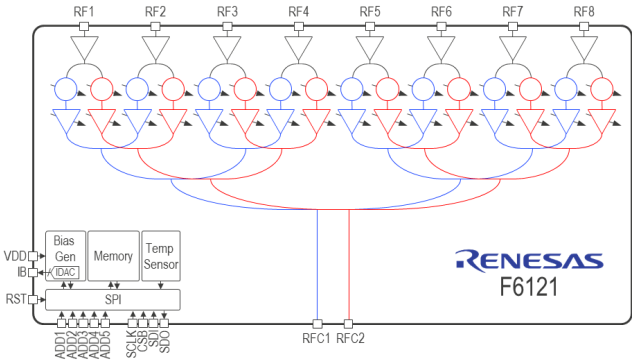

Figure 1. Block Diagram

Features

- Frequency: 10.7 to 12.75 GHz
- Electronic gain control: -17.7 to 10.7dB
  - Step size: 0.45dB
  - RMS gain error: 0.17dB
- 360° phase control
  - Step size: 5.6°
  - RMS phase error: 1.5°
- Input P1dB: -32dBm
- Noise figure: 6.1dB
- Channel-to-channel isolation: 37dB
- Low power consumption
  - Single-beam mode: 34.5mW/ch
  - Dual-beam mode: 29.2mW/ch
  - Low Bias mode for 19% reduction
  - Standby mode: 6.2mW
- Single supply voltage operation
  - VDD: 2.1 to 2.5V
  - Internal LDO: 1.8V
- Fast and flexible digital interface
  - 4-wire SPI up to 50MHz
  - 5-bit address for 32 devices per SPI bus
  - Fast beam steering with 128-state memory
  - 50ns phase and gain settling time
- Compact size for planar integration on λ/2 grid
  - 4.6 × 3.8 × 0.9 mm, 63-FCCSP
- Ambient operating temperature: -40°C to +85°C

Note: Performance is typical at 11.7GHz. For more information, see Specifications and Typical Performance Characteristics sections.

Applications

- Electronically Steered Phased Array Antennas (ESAs)
- Aerospace, Maritime, and Satcom-on-the-move (SOTM)
- Ku-Band SATCOM Terminals

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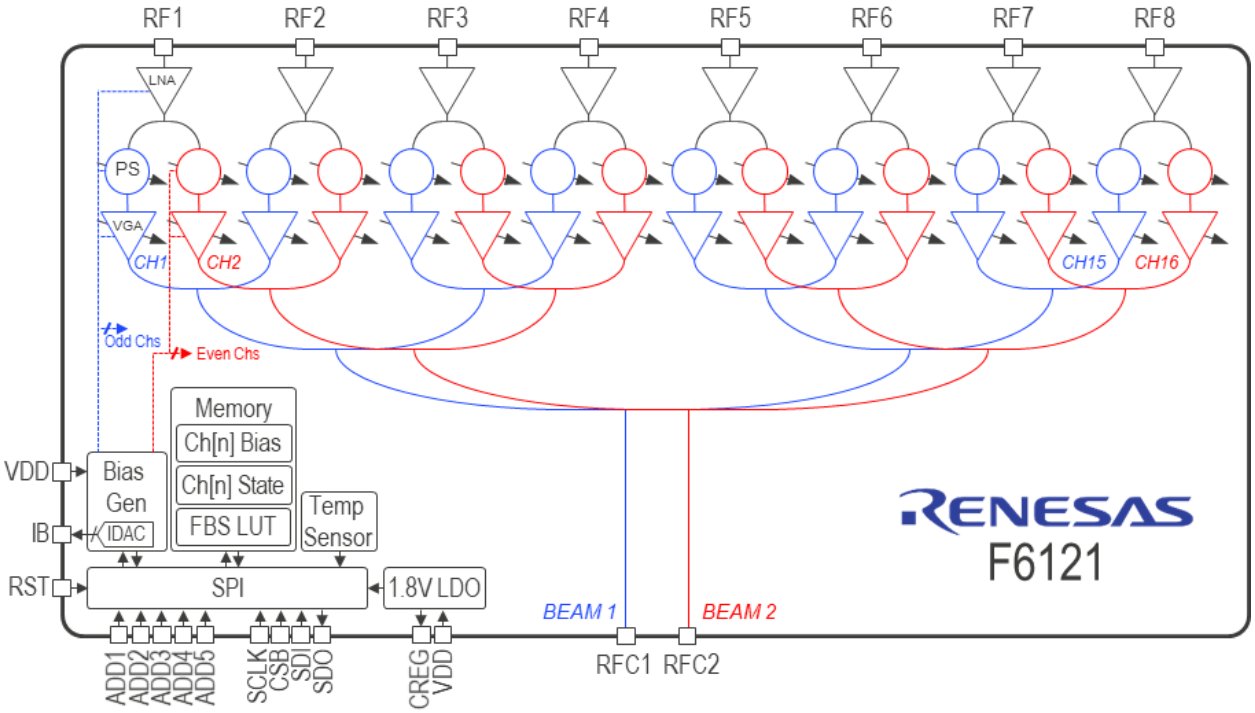
1. Block Diagram



2. Pin Information

2.1 Pin Assignments

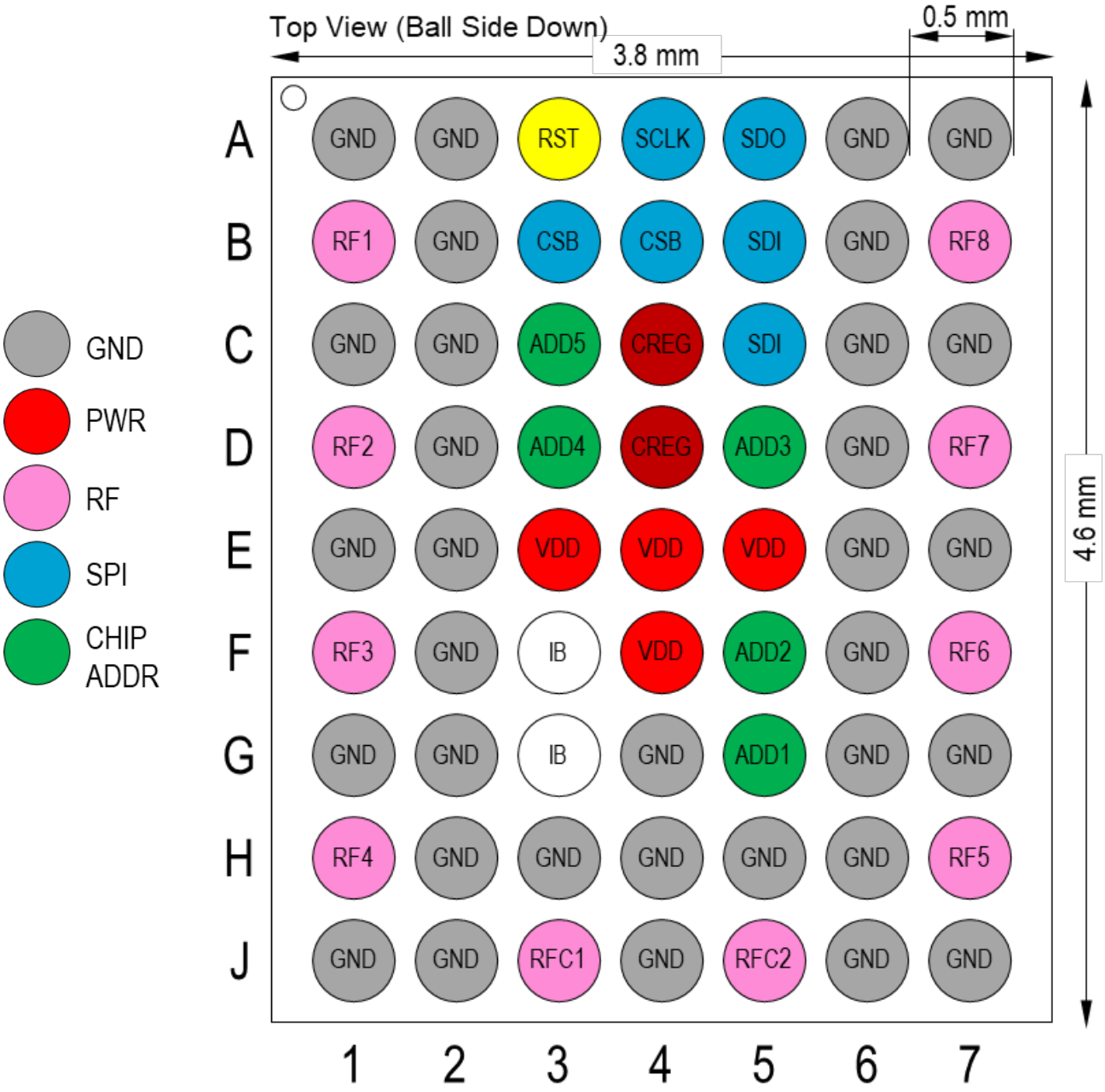


Figure 2. Pin Assignments – Top View

2.2 Pin Descriptions

Pin Number	Name	Type	I/O [1]	Description
A1, A2, A6, A7, B2, B6, C1, C2, C6, C7, D2, D6, E1, E2, E6, E7, F2, F6, G1, G2, G4, G6, G7, H2, H3, H4, H5, H6, J1, J2, J4, J6, J7	GND	Ground	-	Power supply ground, common for RF, DC, and Digital.
E3, E4, E5, F4	VDD	Power	Input	Positive supply voltage input.
C4, D4	CREG	Power	Output	Digital supply voltage LDO regulator node. [2]
A3	RST	Digital	Input (PU)	Resets all memory registers to factory default. Active low.
A4	SCLK	Digital	Input (PD)	SPI clock input.
B3, B4	CSB	Digital	Input (PU)	SPI chip-select bar.
A5	SDO	Digital	Output	SPI data output.
B5, C5	SDI	Digital	Input (PD)	SPI data input.
G5	ADD1	Digital	Input (PU)	Chip address bits. ADD5 is the MSB and ADD1 is the LSB in ADD[4:0] of the SPI command word. Connect to GND for logic 0, leave floating or connect to 1.8V for logic 1.
F5	ADD2	Digital	Input (PU)	
D5	ADD3	Digital	Input (PU)	
D3	ADD4	Digital	Input (PU)	
C3	ADD5	Digital	Input (PU)	
J3	RFC1	Analog	Output	RF output common port for beam 1
J5	RFC2	Analog	Output	RF output common port for beam 2
B1	RF1	Analog	Input	RF input port 1 driving channels 1 and 2. [3]
D1	RF2	Analog	Input	RF input port 2 driving channels 3 and 4. [3]
F1	RF3	Analog	Input	RF input port 3 driving channels 5 and 6. [3]
H1	RF4	Analog	Input	RF input port 4 driving channels 7 and 8. [3]
H7	RF5	Analog	Input	RF input port 5 driving channels 9 and 10. [3]
F7	RF6	Analog	Input	RF input port 6 driving channels 11 and 12. [3]
D7	RF7	Analog	Input	RF input port 7 driving channels 13 and 14. [3]
B7	RF8	Analog	Input	RF input port 8 driving channels 15 and 16. [3]
F3,G3	IB	Analog	Output	Programmable IDAC analog output for external LNA biasing

1. Pull-up (PU) or pull-down (PD) resistors, if applicable, are indicated in parentheses. Resistor value in either case is 309kΩ
2. Requires a low impedance (<0.1Ω) connection to GND through a 10uF external capacitor.
3. Outputs from odd channels are combined into output RFC1 (Beam 1). Outputs from even channels are combined into output RFC2 (Beam 2).

3. Specifications

Exposure of the device to parameter values outside of the range listed below may reduce the operating lifetime and adversely and permanently alter the device characteristics. Furthermore, functional operation at or near absolute maximum ratings is not implied.

3.1 Absolute Maximum Ratings

Parameter	Symbol	Conditions	Minimum	Maximum	Unit
Supply Voltage	V_{DD}		-0.3	3.0	V
RF Input Power	P_{IN}	V_{DD} ≤ 2.5V, VSWR < 2:1		-5	dBm
Junction Temperature	T_J			150	°C
ESD – Human Body Model	V_{HBM}	JS-001-2012		2,500	V
ESD – Charged Device Model	V_{CDM}	JESD22-C101		250	V

3.2 Thermal Information

Parameter	Symbol	Value	Unit
Theta JB. Junction to board.	θ_{JB}	2.5	°C/W
Theta JC. Junction to case. (case top)	θ_{JC}	22	°C/W
Theta JA. Junction to ambient.	θ_{JA}	28	°C/W
Storage Temperature	T_{STOR}	-40 to +150	°C
Lead Temperature (soldering, 30s)	T_{LEAD}	260	°C

3.3 Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit
RF Frequency Range	f_{RF}	10.7		12.75	GHz
Power Supply Voltage	V_{DD}	2.1	2.3	2.5	V
Ambient Temperature	T_A	-40		85	°C
RF Pin Load Impedance	Z_{RF}		50		Ω

3.4 Electrical Specifications

Unless stated otherwise, all specifications below are for V_{DD} = 2.3V, T_A = 25°C, f_{RF} = 11.7 GHz and nominal bias register values. All channels are powered ON and programmed identically. Parameters are measured using the Evaluation Kit Circuit with trace and connector losses de-embedded and $Z_S = Z_L = 50\Omega$ on all ports.

3.4.1. DC Electrical Specifications

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Supply Current, Power Down State	I_{DD_PWRDN}	All channels disabled and bias generator disabled		2.1		mA
Supply Current, Standby State	I_{DD_STBY}	All channels disabled		2.7		mA
Supply Current, Single-beam Mode	I_{DD_SB}	8 of 16 channels enabled		120		mA
Supply Current, Dual-beam Mode	I_{DD_DB}	All channels enabled		203		mA

3.4.2. Digital Electrical Specifications

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Input High Voltage	V_{IH}	F_{CLK} = 1 MHz	***1.5*** [1]			V
		F_{CLK} = 10 MHz	***1.5***			V
		F_{CLK} = 25 MHz	***1.65***			V
Input Low Voltage	V_{IL}	F_{CLK} = 1 MHz			***0.35***	V
		F_{CLK} = 10 MHz			***0.35***	V
		F_{CLK} = 25 MHz			***0.25***	V
High and Low Input Current	I_{IH}, I_{IL}		***-100***		***100***	µA
Output High Voltage	V_{OH}	I_{OH} = -2mA	***1.1***			V
Output Low Voltage	V_{OL}	I_{OL} = 2mA			***0.5***	V
SPI Clock Frequency	F_{CLK}				***50*** [2]	MHz

1. Parameters in bold italic are confirmed by test.
2. Tested with 0V / 1.8V for V_{IL} / V_{IH}.

3.4.3. RF Electrical Specifications

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Gain	G_{MAX}	Electronic Gain[1] at max gain setting		10.7		dB
Gain Flatness vs. Frequency	G_{VAR_FREQ}	f_{RF} = 10.7 - 12.75 GHz		3.4		dB
Gain Variation vs. Temperature	G_{VAR_TEMP}	T_A = -40°C - 85°C		6.2 [2]		dB
Noise Figure	NF			6.1		dB
NF Variation vs. Temperature	NF_{VAR_TEMP}	T_A = -40°C - 85°C		1.8		dB
Input 1dB Compression Point	IP1dB			-32		dBm
Out-of-band IP1dB	$IP1dB_{OOB}$	f_{RF} = 13.75 - 14.5 GHz		-24		dBm
Input Third Order Intercept Point	IIP3	Pin = -35 dBm/tone, Δf = 1MHz		-23		dBm
Input Return Loss	IRL	f_{RF} = 10.7 - 12.75 GHz		13		dB
Output Return Loss	ORL	f_{RF} = 10.7 - 12.75 GHz		14		dB
Phase Control						
Phase Adjustment Range	Φ_{RANGE}			360		deg
Phase Adjustment Step	Φ_{STEP}			5.6		deg
RMS Phase Error	Φ_{ERR_RMS}			1.5		deg
RMS Gain Error Over Phase Settings	$G_{ERR\_RMS\_PH}$			0.32		dB
Gain Control						
Gain Adjustment Range	G_{RANGE}			28.4		dB
Gain Adjustment Step	G_{STEP}			0.45		dB
RMS Gain Error, Upper Range	$G_{ERR\_RMS\_U}$	Gain codes 32 - 63		0.17		dB
RMS Gain Error, Lower Range	$G_{ERR\_RMS\_L}$	Gain codes 0 - 31		0.28		dB
RMS Phase Error Over Gain Setting, Upper Range	$\Phi_{ERR\_G\_U}$	Gain codes 32 - 63		0.9		deg
RMS Phase Error Over Gain Setting, Lower Range	$\Phi_{ERR\_G\_L}$	Gain code 0 - 31		1.8		deg
Channel to Channel Isolation						
Phase Variation Over Adjacent Ch Phase Setting	$\Phi_{VAR\_ADJ\_CH}$	Adjacent Ch on Same beam		1.7		deg
Phase Variation Over Adjacent Ch Phase Setting	$\Phi_{VAR\_ADJ\_BM}$	Adjacent Ch on Adjacent Beam		0.7		deg
Adjacent Channel Isolation	$ISO_{CH\text{-}CH}$	f_{RF} = 10.7 - 12.75 GHz		37		dB

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Disabled Channel Isolation	ISO_{IN_OUT}	f_{RF} = 10.7 - 12.75 GHz Channel Disabled		47		dB
Reverse Isolation	ISO_{OUT_IN}	f_{RF} = 10.7 - 12.75 GHz		54		dB

1. Electronic gain is defined as the Single Path Gain (SPG) + 9dB. SPG is the measured gain (S21) between one of the eight input ports and the common port, with the other seven Rx ports match terminated.
2. With PTAT bias profile. A steeper bias current compensation profile from PTAT2 can improve the gain flatness. For more information, see Typical Performance Characteristics and PTAT and PTAT2 Temperature Compensation Modes.

4. Typical Application Circuit

Figure 3 shows a typical polarization agile phased array antenna system schematic using the F6121. Each F6121 is driven by four dual-polarized patch antenna elements. An F6921 dual-ch low noise amplifier is also shown placed between the patch antenna and the F6121 BFIC to reduce the receive noise figure and increase the antenna G/T. The F6921 LNA requires a separate voltage (not shown) of 0.95V nominal and a bias/control current from the F6121. The F6121 is used to set the receive polarization and the beam pointing direction for the four antenna elements. A grouping of F6121 devices (up to 32) that share the same 4-wire SPI bus form a sub-array. Each F6121 has a unique address within a sub-array. Multiple sub-arrays are further combined to form a complete phased array antenna system. For single-beam systems, only the beam 1 output should be used, leaving the beam 2 output match terminated or open.

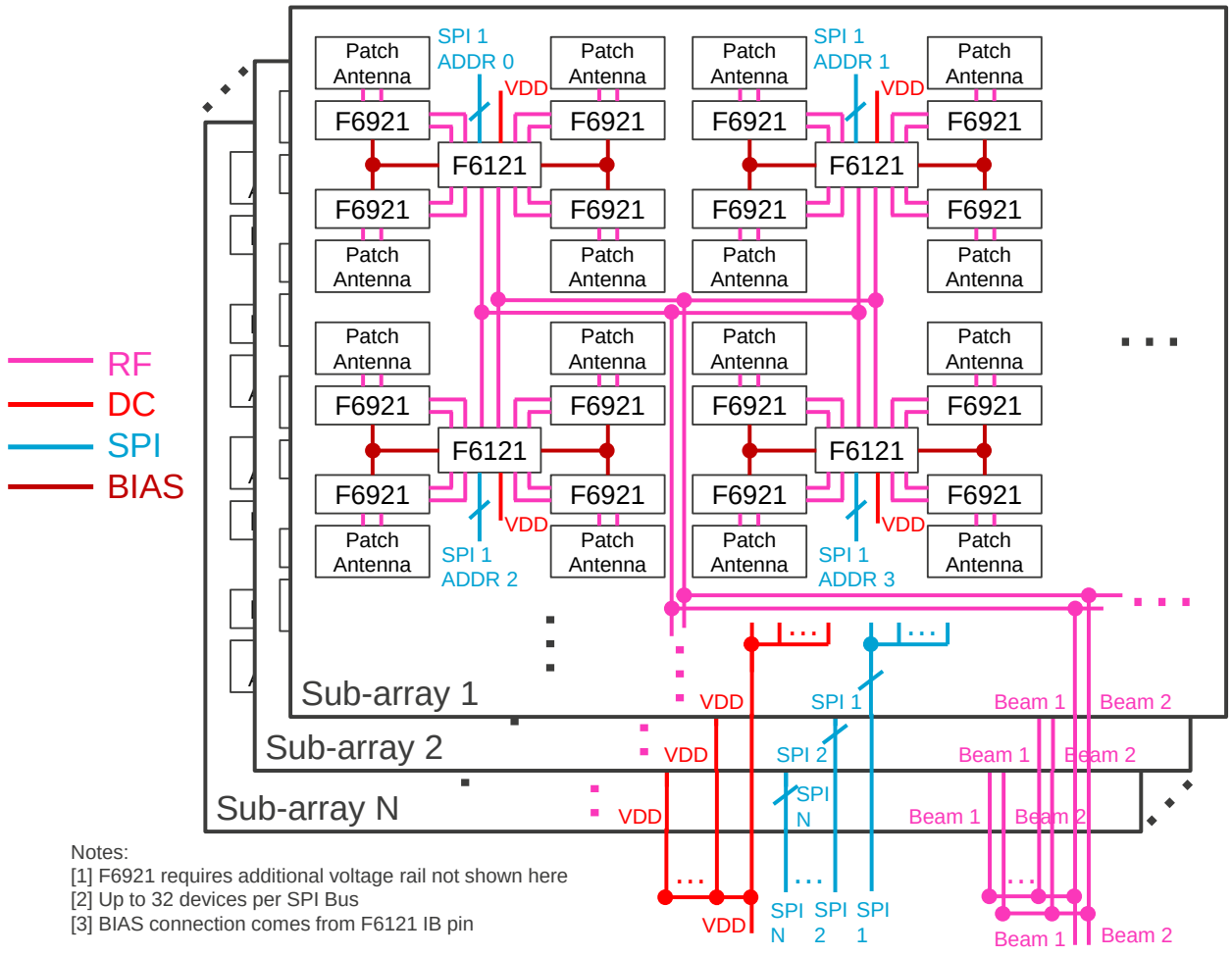


Figure 3. Typical Application Circuit Schematic

Figure 4 shows a typical 4×4 sub-array layout. The antenna elements are arranged on a periodic grid and spaced λ/2 apart at the highest frequency of operation F_{max}, where λ is the free-space wavelength at F_{max}. This spacing is a necessary condition for grating-lobe free performance over a hemispherical scan volume. A more constrained scan volume may allow relaxation of the periodic spacing up to λ, which allows for fewer antenna elements and BFICs to realize a given antenna gain. The F6921 LNAs are placed in close proximity to the antenna feeds to minimize the feed losses, which reduces the noise figure and increases G/T. This layout uses a square array grid for ease of routing, but other configurations such as a triangular grid can be accommodated with a moderate increase in routing complexity.

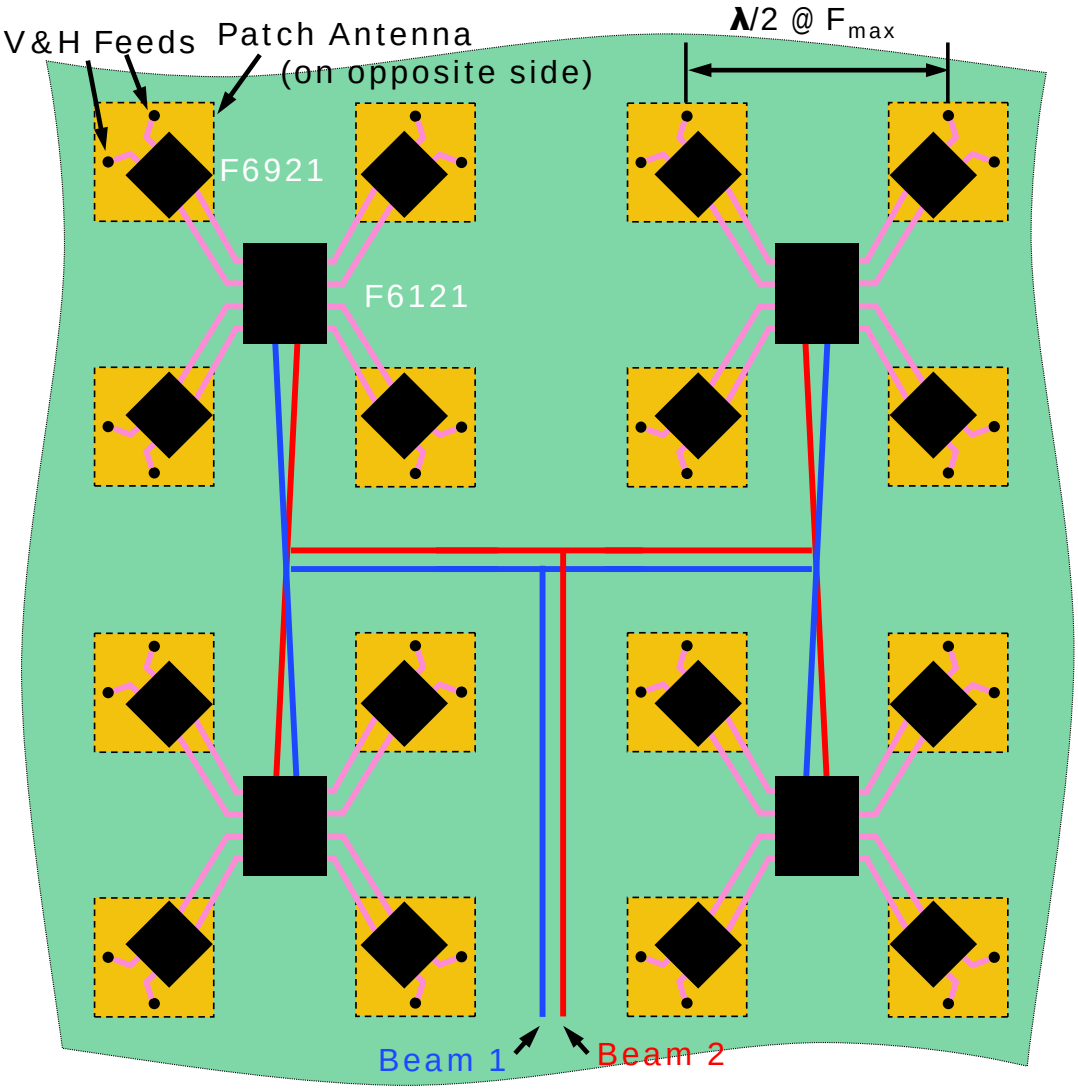


Figure 4. Typical Application Circuit Layout

5. Typical Performance Characteristics

Except when swept or indicated otherwise, the following conditions apply: V_{DD} = 2.3V, T_A = 25°C, f_{RF} = 11.7GHz, all registers are set to their typical values, all channels are enabled and programmed identically, $Z_S = Z_L = 50\Omega$ on all RF ports.

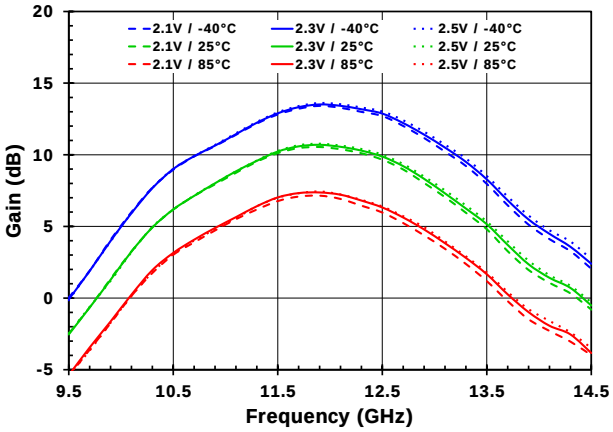


Figure 5. Electronic Gain

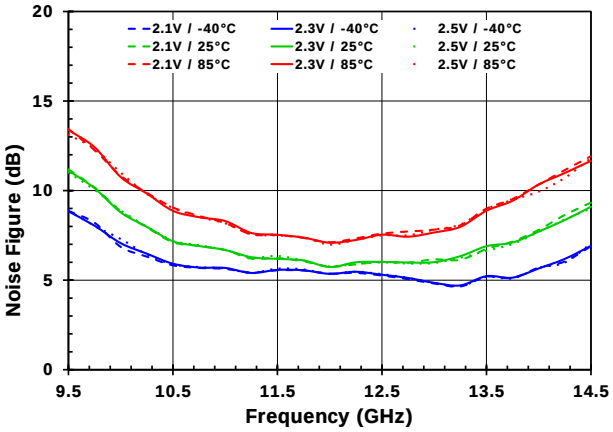


Figure 6. Noise Figure

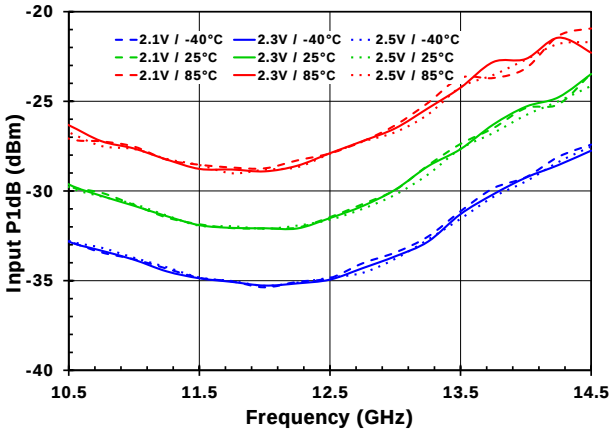


Figure 7. Input 1dB Compression

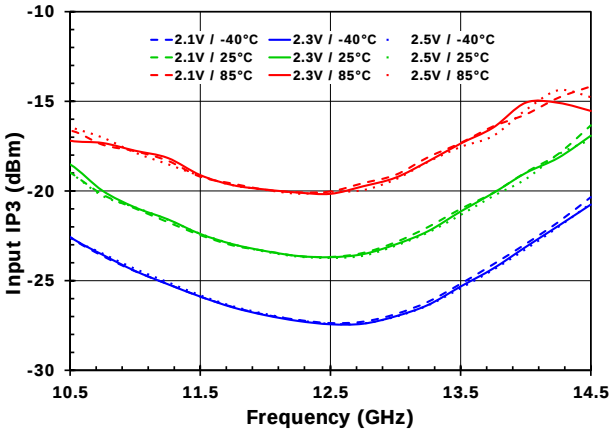


Figure 8. Input 3rd Order Intercept

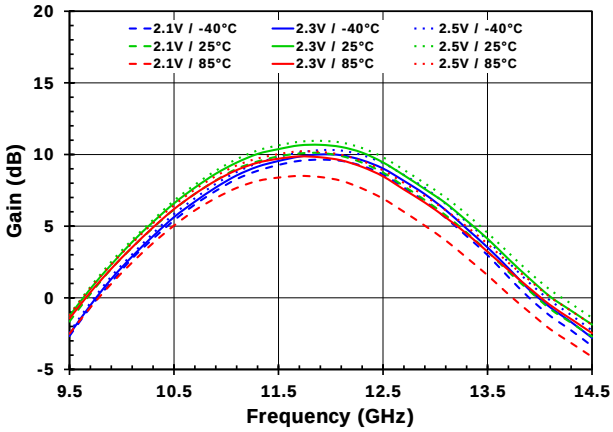


Figure 9. Electronic Gain with PTAT2

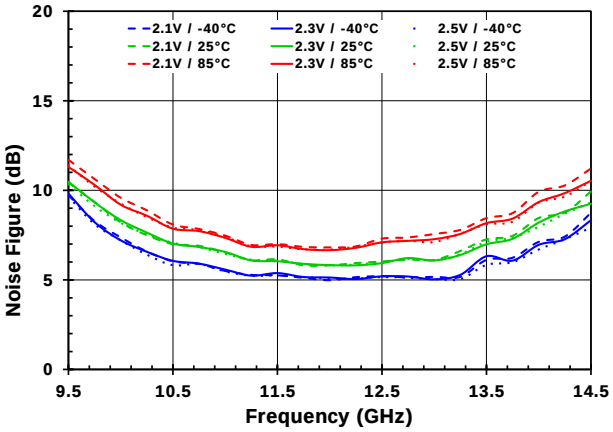


Figure 10. Noise Figure with PTAT2

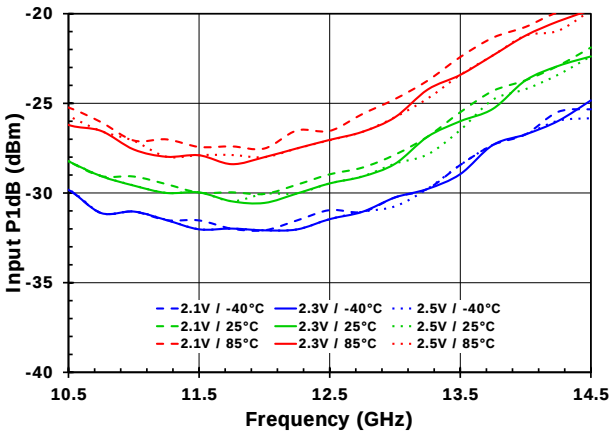


Figure 11. Input 1dB Compression with PTAT2

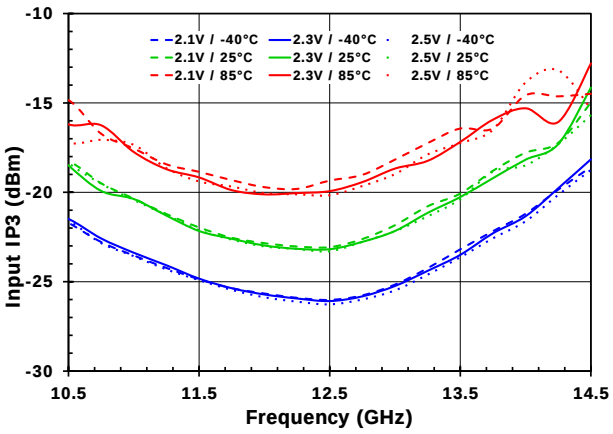


Figure 12. Input 3rd Order Intercept with PTAT2

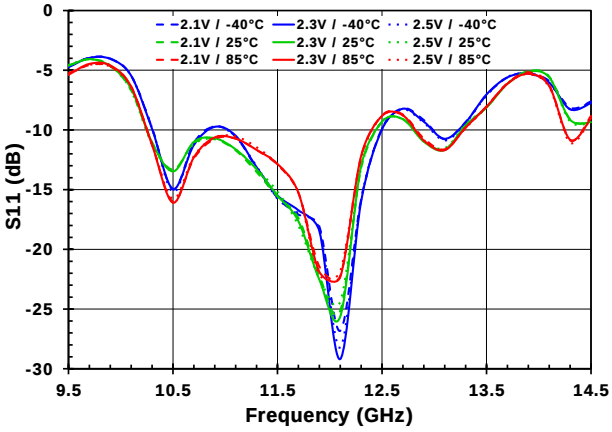


Figure 13. Input Match

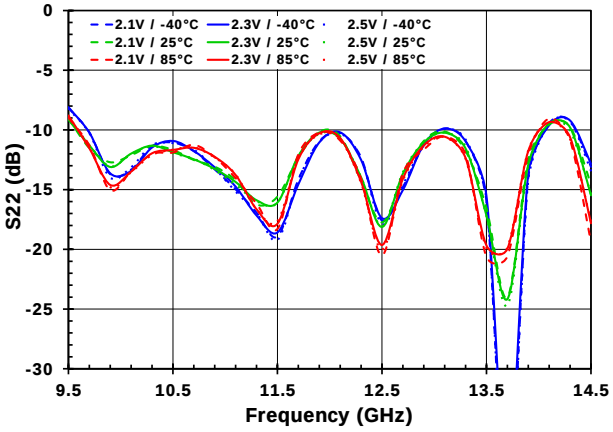


Figure 14. Output Match

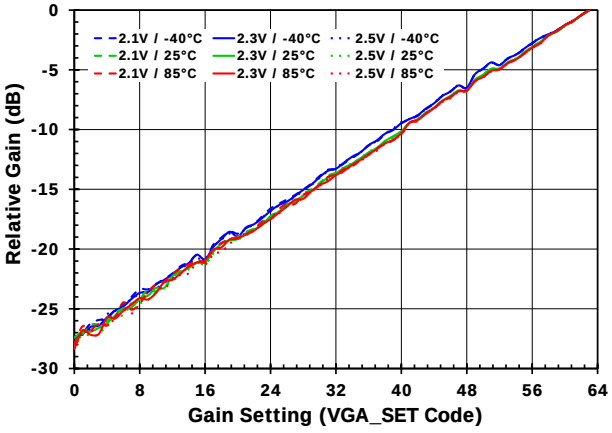


Figure 15. Gain vs. Gain Setting

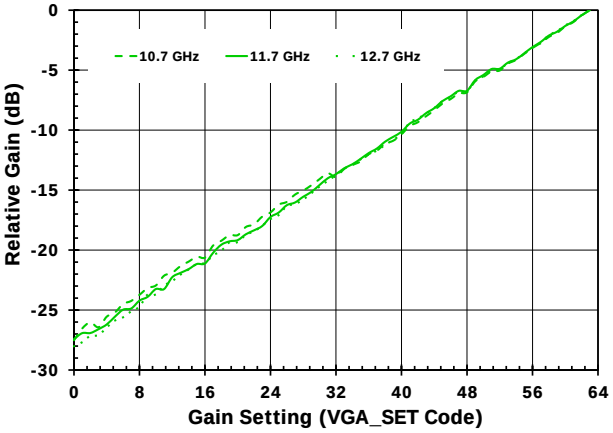


Figure 16. Gain vs. Gain Setting and Frequency

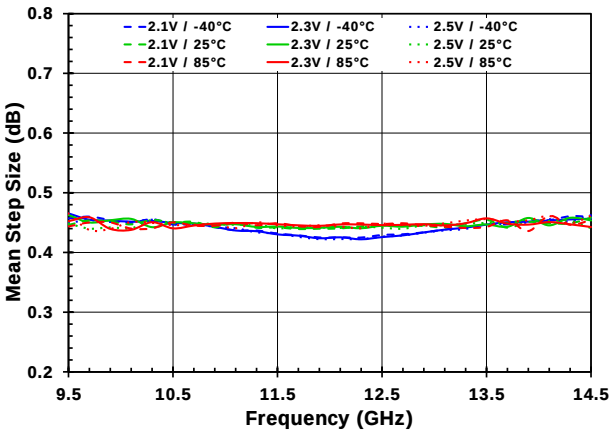


Figure 17. Mean Gain Change Per Code Step, VGA_SET Code = 32-63

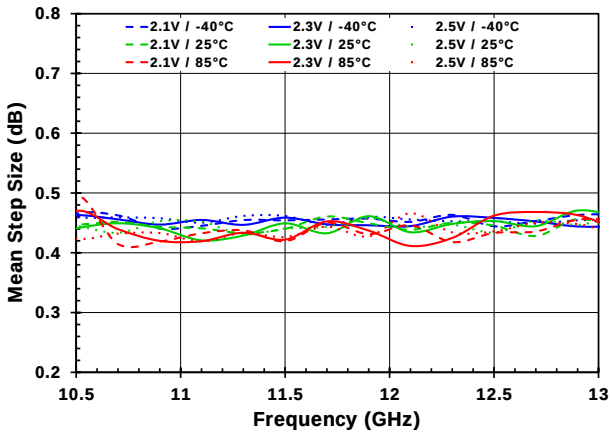


Figure 18. Mean Gain Change Per Code Step, VGA_SET Code = 0-31

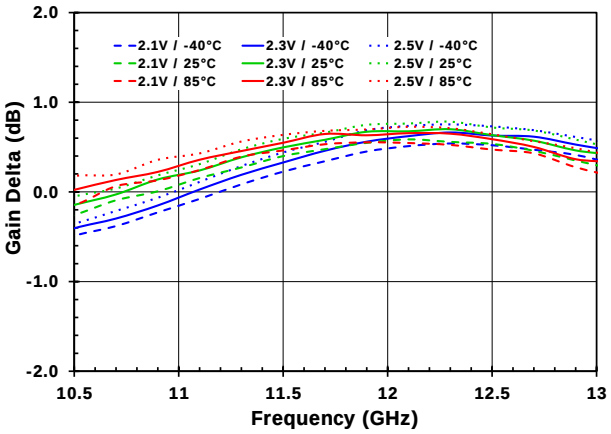


Figure 19. Gain Change at VGA_SET Code 31→32 Transition

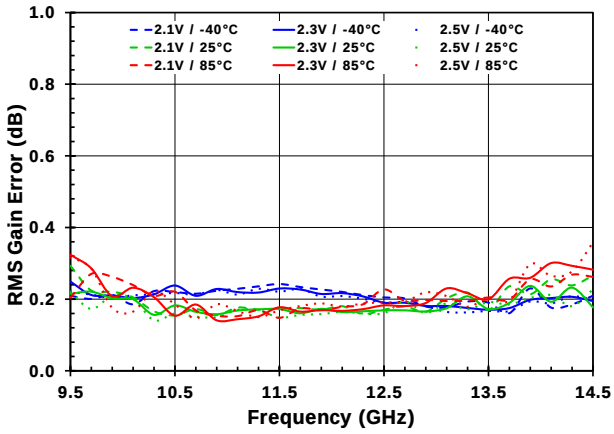


Figure 20. RMS Gain Error over Upper Gain Settings, VGA_SET Codes = 32-63

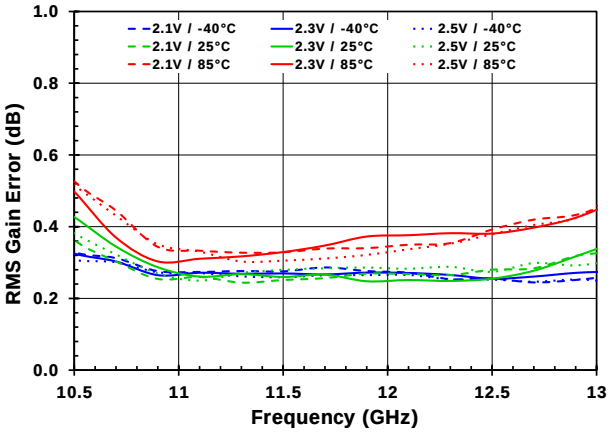


Figure 21. RMS Gain Error over Lower Gain Settings, VGA_SET Codes = 0-31

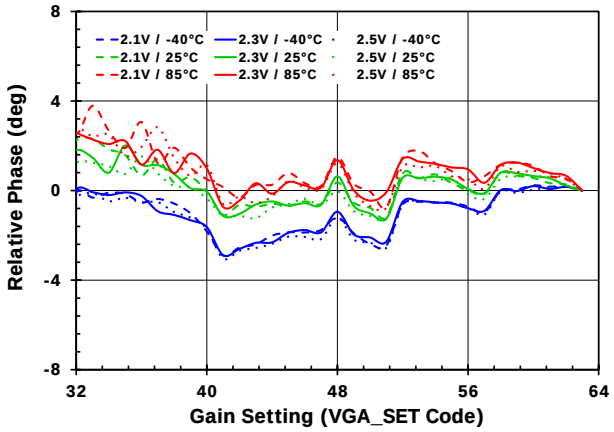


Figure 22. Phase vs. Gain Setting, Upper Gain Settings, VGA_SET Codes = 32-63

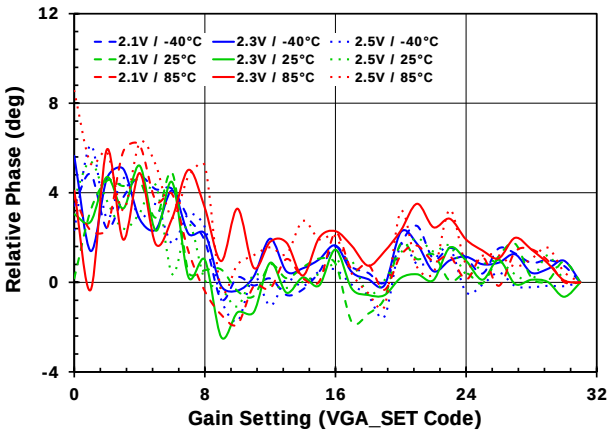


Figure 23. Phase vs. Gain Setting, Lower Gain Settings, VGA_SET Codes = 0-31

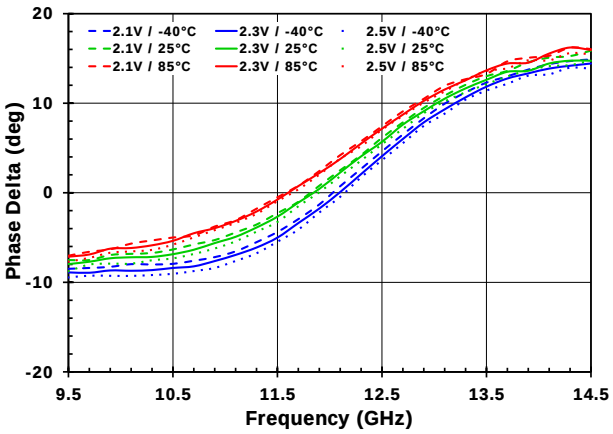


Figure 24. Phase Change at VGA_SET Code 31→32 Transition

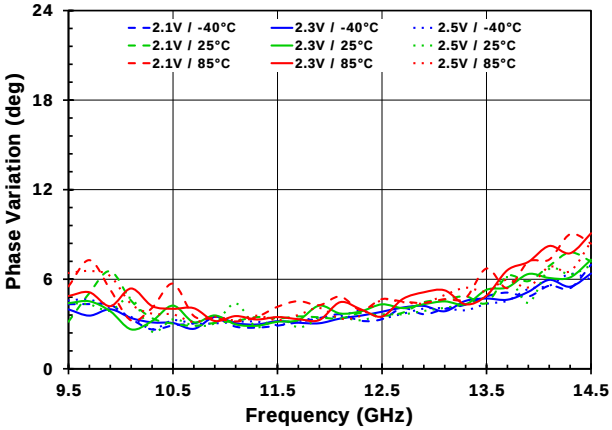


Figure 25. Max-to-min Phase Variation over All Upper Gain Settings (VGA_SET Codes 32-63)

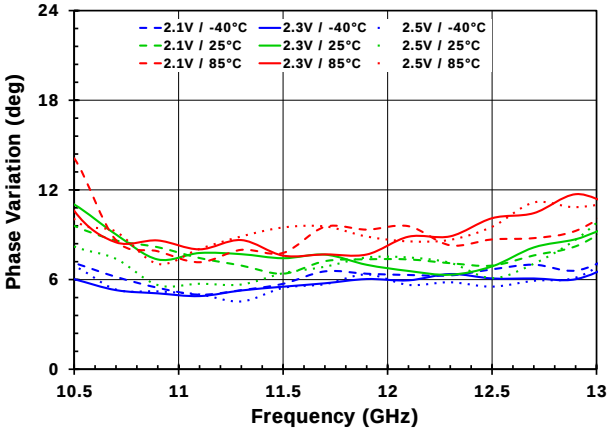


Figure 26. Max-to-min Phase Variation over All Lower Gain Settings (VGA_SET Codes 0-31)

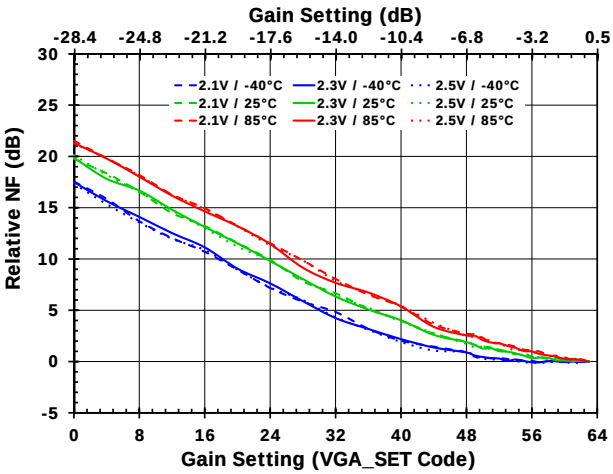


Figure 27. Noise Figure Change with Gain Setting

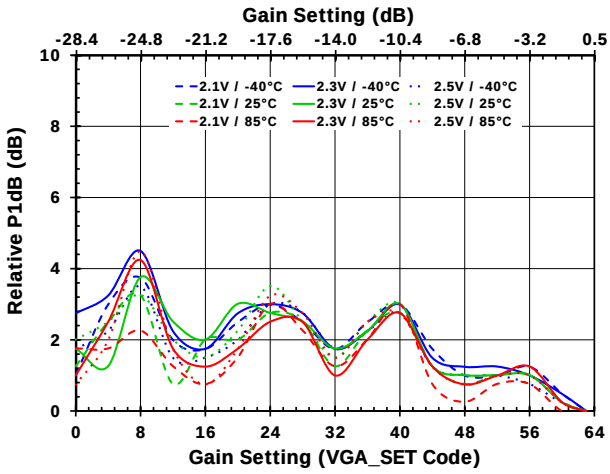


Figure 28. Input 1dB Compression Change with Gain Setting

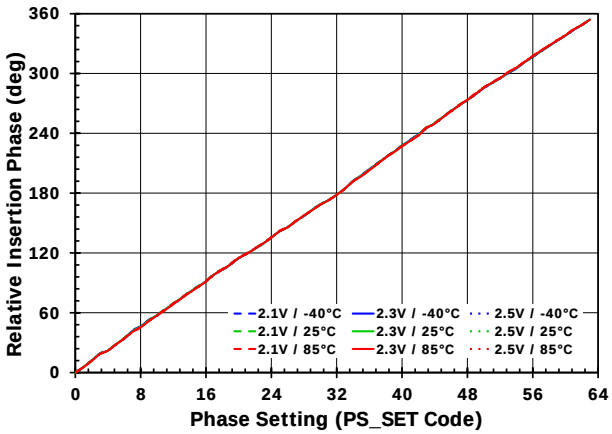


Figure 29. Insertion Phase vs. Phase Setting

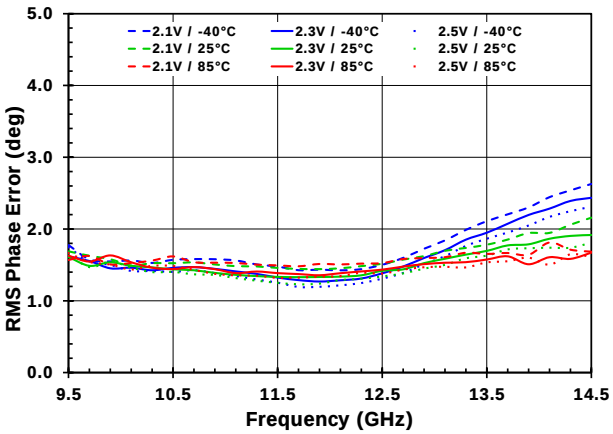


Figure 30. RMS Phase Error over All Phase Settings

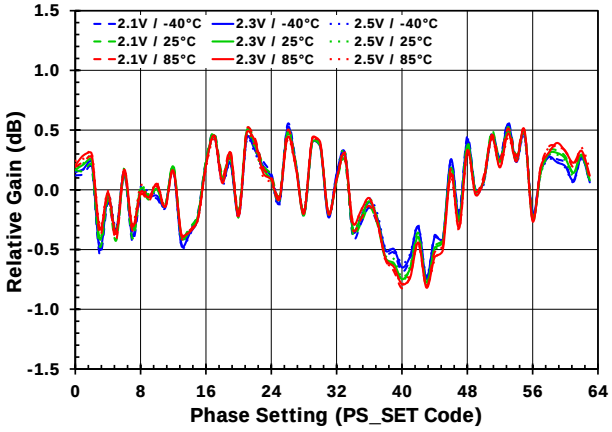


Figure 31. Gain Variation with Phase Setting

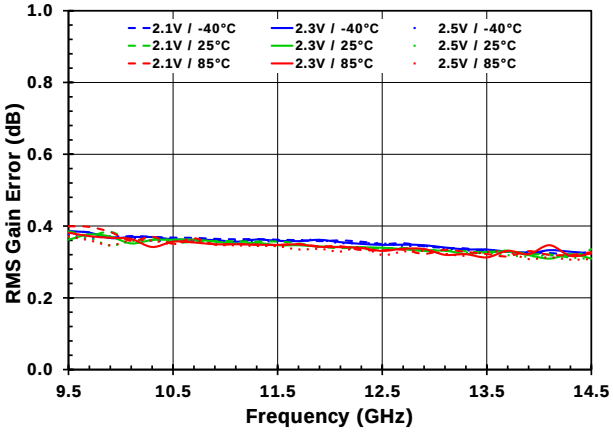


Figure 32. RMS Gain Error over All Phase Settings (PS_SET Codes 0-63)

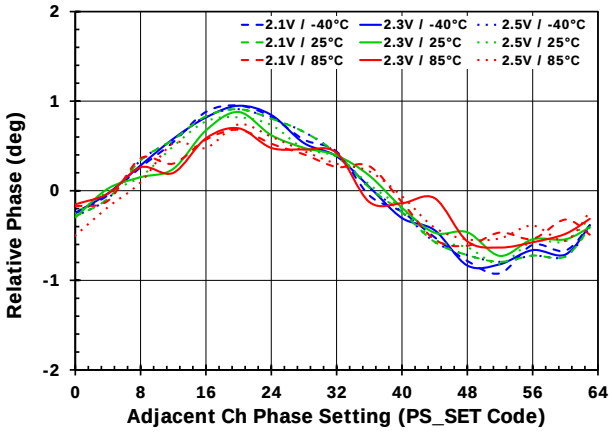


Figure 33. Phase Variation with Adjacent Channel Phase Setting

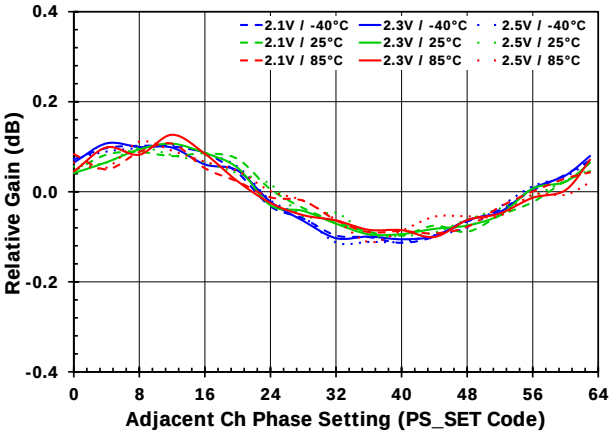


Figure 34. Gain Variation with Adjacent Channel Phase Setting

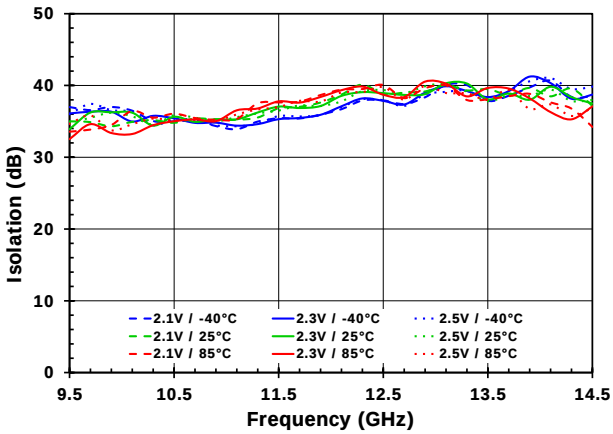


Figure 35. Channel to Channel Isolation, Adjacent Channel on Same Beam

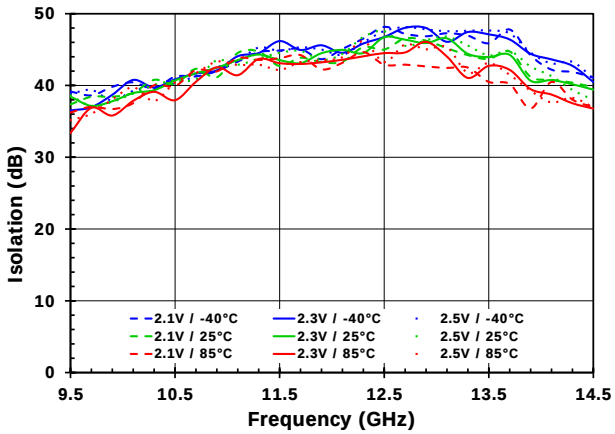


Figure 36. Channel to Channel Isolation, Adjacent Channel on Adjacent Beam

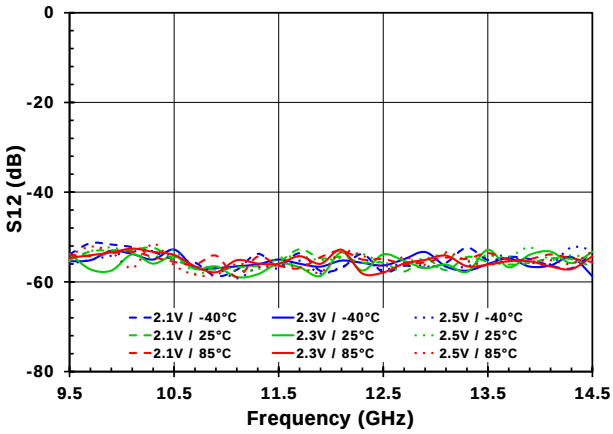


Figure 37. Reverse Isolation

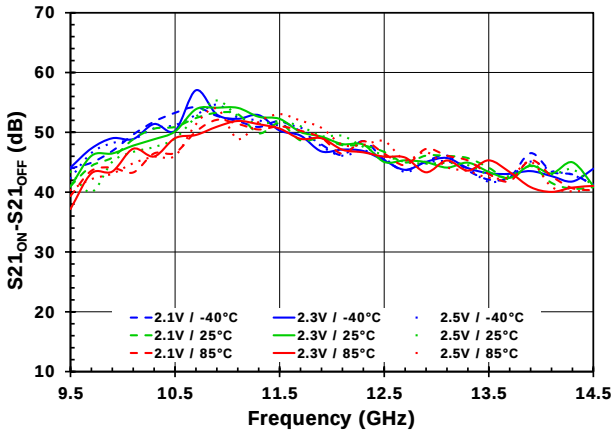


Figure 38. Disabled Channel Isolation

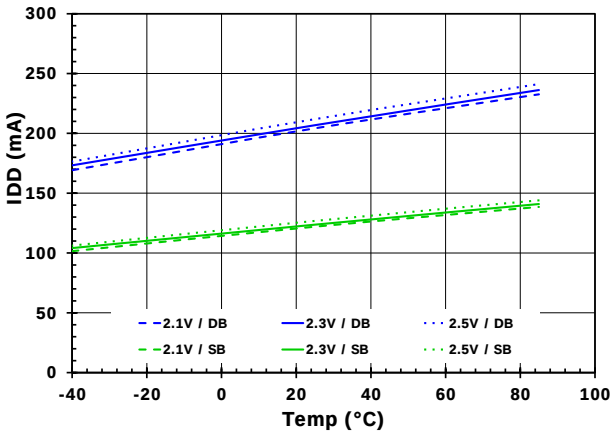


Figure 39. Current Consumption

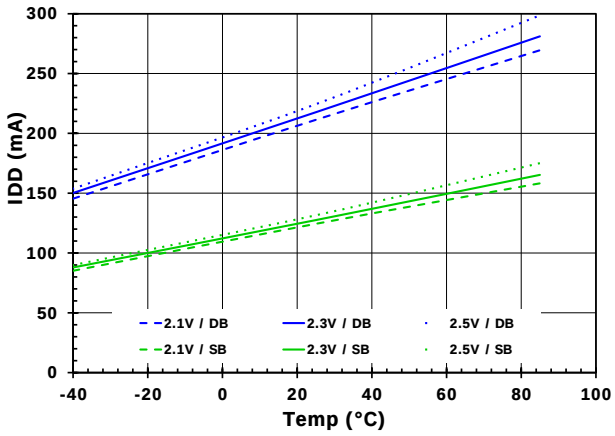


Figure 40. Current Consumption with PTAT2

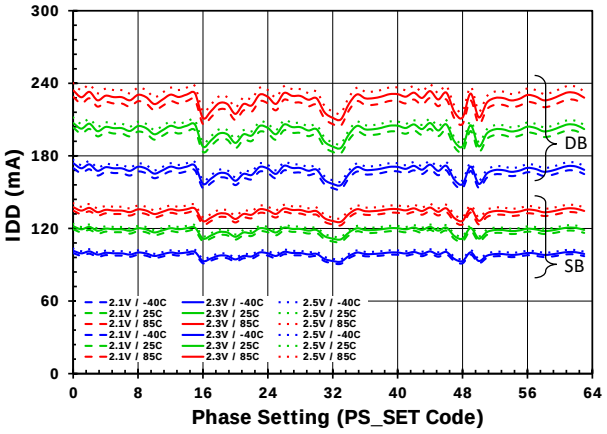


Figure 41. Current Consumption vs. Phase Setting

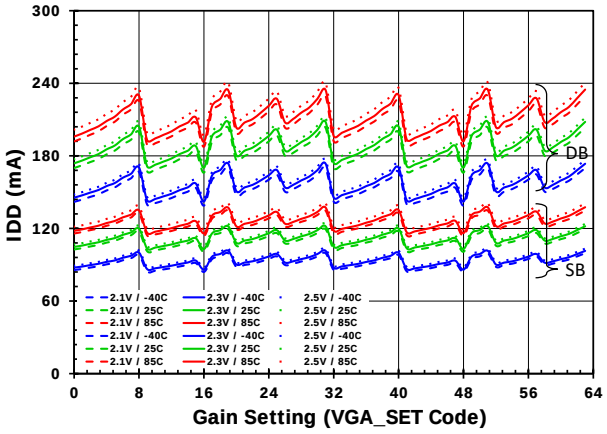


Figure 42. Current Consumption vs. Gain Setting

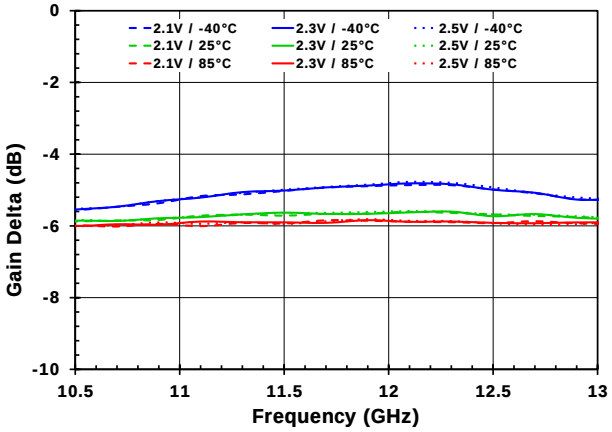


Figure 43. Gain Change with LNA Bypassing (LNA_SW 1→0)

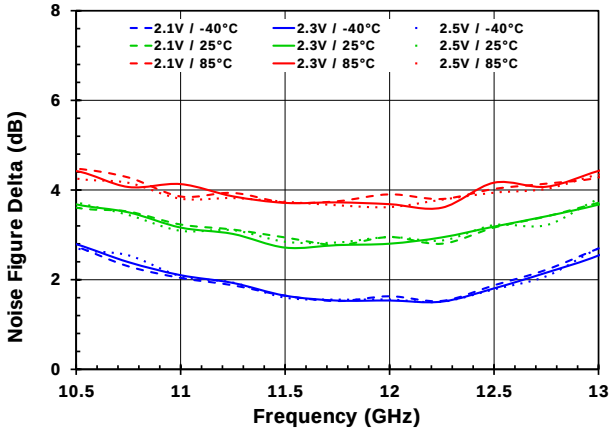


Figure 44. Noise Figure Change with LNA Bypassing (LNA_SW 1→0)

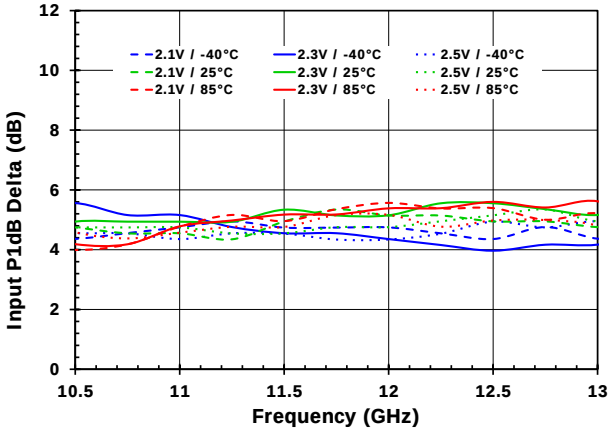


Figure 45. Input 1dB Compression Change with LNA Bypassing (LNA_SW 1→0)

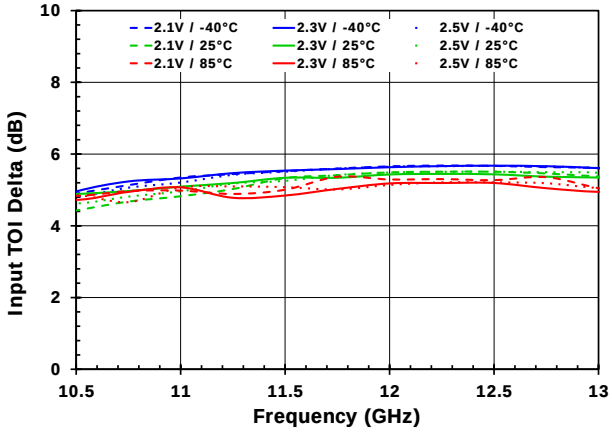


Figure 46. Input Third Order Intercept Change with LNA Bypassing (LNA_SW 1→0)

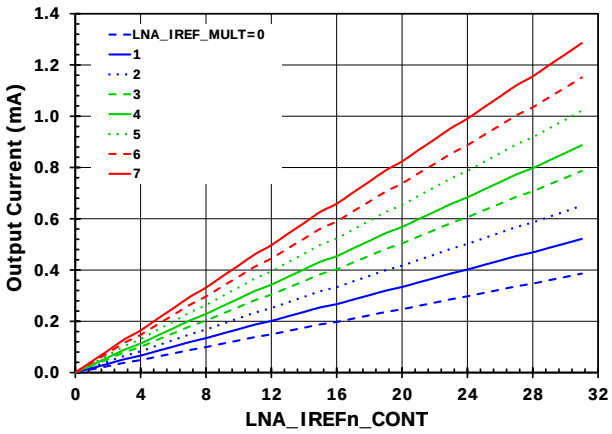


Figure 47. IB Pin Output Current vs. IDAC Code Setting (V_{LOAD} = V_{IB} = 0.8V)

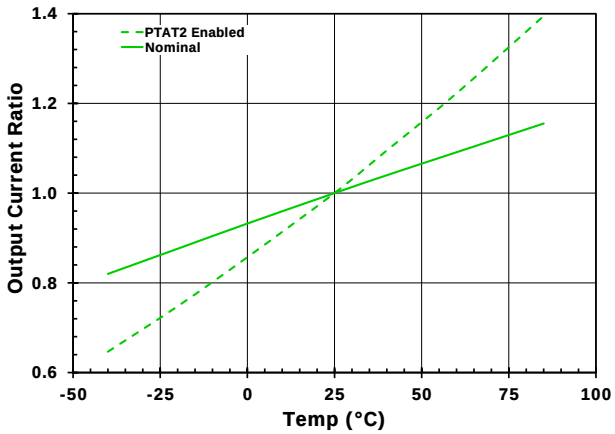


Figure 48. IB Pin Output Current Variation with Temperature

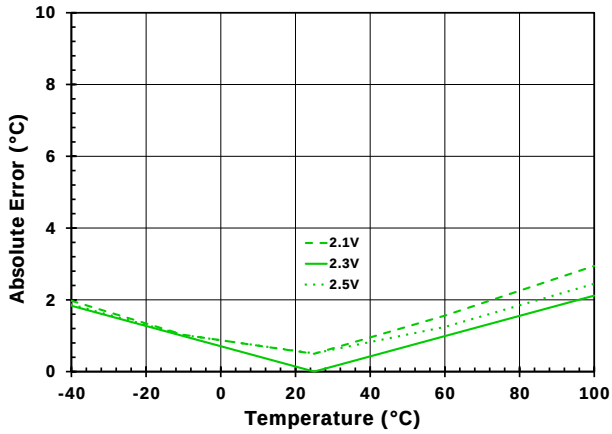


Figure 49. Temperature Sensor Error

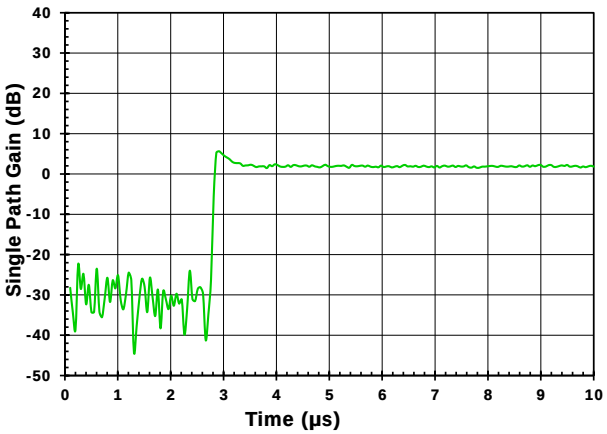


Figure 50. Channel Standby to Active Transient Response

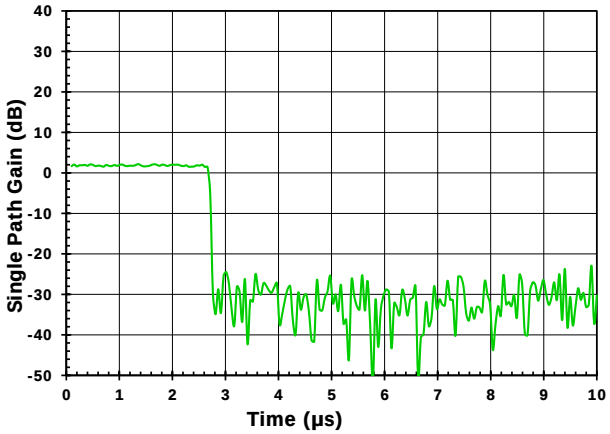


Figure 51. Channel Active to Standby Transient Response

6. Feature Description

6.1 Dual-beam Operation

The F6121 can be operated in dual-beam (default) or single-beam mode. The device can be configured for single beam operation by writing a 0 to the CH_PWD field of the CHn_SET of all of the even channels (n=2,4,…,16). RFC1 becomes the combined output port in single-beam operation. It is important to note that disabling the even channels by writing the CH_PWD field does NOT disable the common Driver Amp (DA), and therefore results in signal reduction only at the RFC2 port with the signal strength at RFC1 unaffected. However, when writing to the CH_PWD field of the odd channels, the Driver Amp (DA) WILL BE disabled resulting in significantly reduced signal output at both RFC1 and RFC2.

6.2 Programmable Bias Modes

Programmable bias controls can be used to trade power consumption for gain, noise figure, and P1dB. In particular, the F6121 has a low power bias mode programmable by the CH_MODE field. The typical change in performance parameters for the Low Bias mode relative to the Nominal bias state is shown in Table 1.

Table 1. Supported Bias Configurations

Bias Mode	CH_MODE	SB IDD [mA]	DB IDD [mA]	G [dB]	NF [dB]	IP1 [dB]	IIP3 [dB]
Nominal	1	NOMINAL					
Low	0	-24 (-19%)	-38 (-18%)	-4.7	+0.7	+1.0	+0.8

6.3 Linearity Improvement Switch (LNA_SW)

The LNA_SW control is used to bypass the first amplifier stage, increasing the input compression point at the expense of lower gain. The typical change in performance parameters for the High Linearity mode relative to Nominal state is shown in Table 2.

Table 2. Linearity Improvement with LNA_SW

Linearity Mode	LNA_SW	G [dB]	NF [dB]	IP1 [dB]	IIP3 [dB]
Nominal	1	NOMINAL			
High	0	-5.6	+2.9	+4.5	+5.2

6.4 PTAT and PTAT2 Temperature Compensation Modes

The bias generator is programmable for PTAT or PTAT2 mode operation. In both modes, the bias current is automatically increased with temperature to compensate for the decrease in the beta parameter of the circuit transistors. Both modes also result in similar gain (within ~1dB) and current consumption at 25°C (within ~5%) when using the recommended register settings. However, the PTAT2 profile maintains a flatter gain at the expense of a steeper slope in current consumption vs temperature. The gain flatness and current consumption variation over temperature of a typical device for both modes is shown in Table 3.

Table 3. Linearity Improvement with LNA_SW

Mode	MB_PT2_EN	MB_PT_ADJ	MB_PT2_SLOPE	Gain Flatness vs. Temperature [dB]	IDD Change Relative to 25°C Value	
					-40°C	85°C
PTAT	0	4	Don't Care	6.2	-16%	+14%
PTAT2	1	4	4	0.8	-31%	+29%

6.5 Temperature Sensor

The on-chip integrated temperature sensor has a dynamic range of -40°C to 125°C. A single SPI write command to the ADC_CTRL register triggers the temperature sensor to perform a measurement. The resulting value is stored as a 10-bit code in the TEMP_DATA register and can be read back through the SPI. The output code value can be approximated by a linear function of temperature as C = 1.3 * (T - T0) + C0, where 1.3 is the temperature sensor slope in LSB / °C and C0 is the temperature sensor intercept. While the slope is tightly distributed, the intercept can vary widely from device to device. To remove the error due to variation of the intercept, the temperature sensor must be calibrated, to find C0, using a single-point calibration routine to achieve the best result.

6.5.1. Single-point Temperature Sensor Calibration

With the F6121 in standby mode (to eliminate self-heating), and at a known ambient temperature T0, query the temperature sensor for the value of C0 = TEMP_DATA[9:0]. This value should be stored in off-chip memory for later use. Once the value of C0 is known, the temperature in operation can be determined from the returned code C using the formula T = 1 / 1.3 * (C - C0) + T0, where C0 is the code value that was returned at known ambient calibration temperature T0.

6.6 Fast Beam Steering (FBS) Look-Up Table (LUT)

The LUT is used for the Fast Beam Steering (FBS) Mode, which allows fast beam switching. A single LUT address points to sixteen 16-bit register locations (equivalent to sixteen channels) that contain channel phase, gain, and enable settings. The phase, gain, and enable settings for 1 LUT entry constitute a beam state. The device has 128 available LUT addresses that can be stored on the chip. For more information, see Global Fast Beam Steering Mode.

6.7 Reset (RST Pin)

The asynchronous RST pin resets all registers to their hardware default (“reset”) state and also latches the default state into active memory. In the default state, all channels are disabled (CHn_PWD = 1), global power down is enabled (GLOBAL_PWD = 1) and master bias is disabled (MB_EN = 0).

6.8 Power-on Reset (POR)

A reset signal is sent when power is first applied to the VDD pin.

7. Programming

7.1 Serial Peripheral Interface (SPI)

The four-wire SPI bus is comprised of the following signals: Serial Clock (SCLK), Serial Data In (SDI), Serial Data Out (SDO), and Chip Select Bar (CSB). The SPI clock can operate up to 50MHz and the SCLK pin is associated with the clock signal rising edge. The input data stream (addresses, commands, messages, and data) is received on the SDI pin, while the output data stream is transmitted from the SDO pin. The SDO pin presents a high-Z impedance level when the chip is in listen mode. The CSB pin acts as a chip-select pin. All SPI bus pins are synchronous and compatible with multi-chip connection.

7.2 Write Operation

For each WRITE operation, it is required that CSB be kept logic low and the input sequence be sent with an active SCLK. At the end of each operation, CSB must be set to a logic high to complete the operation. The SDO pin is in high-Z mode during the WRITE operation.

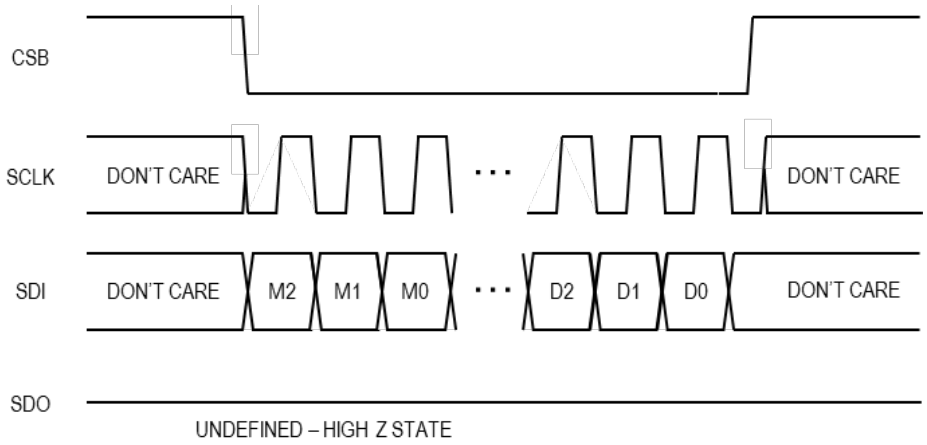


Figure 52. Write Command SPI Sequence

7.3 Read Operation

Register contents can be read back via the SDO pin. For each READ operation, CSB must be kept logic low and the input sequence be sent with an active SCLK. At the end of each operation, CSB must be set to logic high to complete the operation. The READ operation will only be performed if the hard-wired address pins of the device match the ADD[4:0] bits sent in the command word. The SDO pin becomes active during the READ operation and will return the stored data value of the selected register. If more than one chip shares a common SDO line, it should be ensured that only one chip is transmitting signals on the SDO line at any given time.

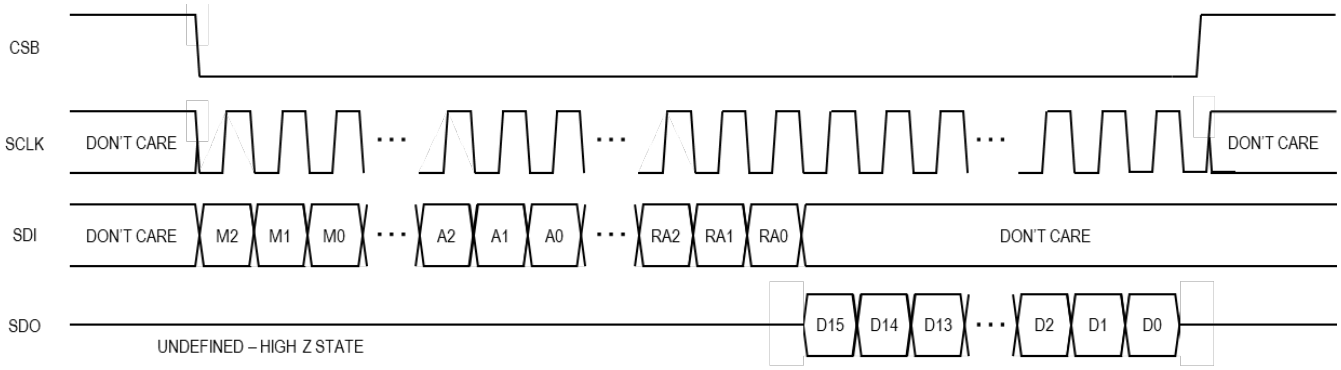


Figure 53. Read Command SPI Sequence

7.4 SPI Timing Requirements

The timing requirements for the WRITE and READ operations are described below. Specifications assume V_{DD} = 2.3V, and 25°C ambient temperature.

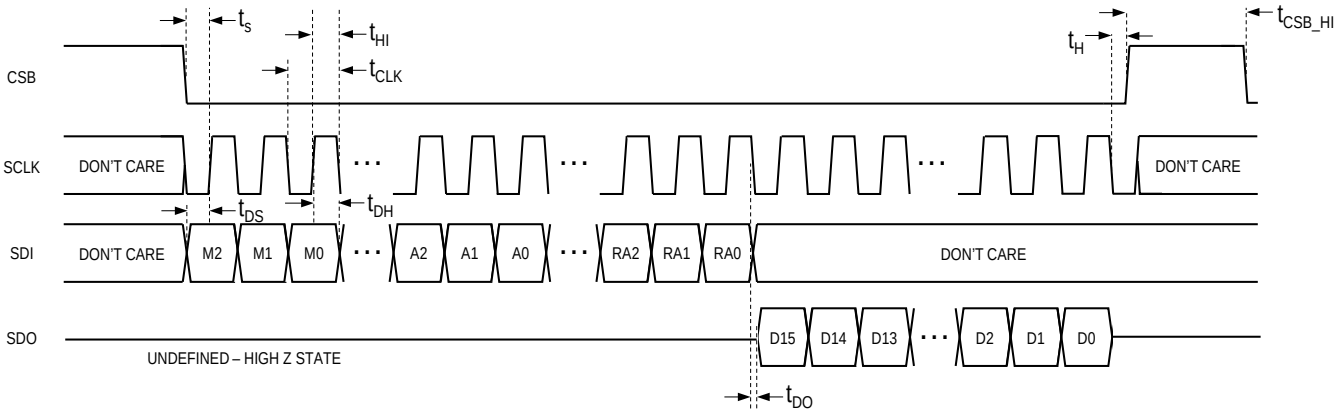


Figure 54. Timing Specifications Diagram

Table 4. SPI Timing Typical Specifications

Symbol	Test Condition	Minimum	Typical	Maximum	Unit
t_S	CSB to SCLK setup time	10			ns
t_{DS}	SDI data setup time	5			ns
t_{DH}	SDI data hold time	5			ns
t_{CLK}	SCLK period	20			ns
t_{HI}	SCLK high time	10			ns
t_{DO}	SCLK falling edge to first valid SDO output bit in a READ operation			15	ns
t_H	SCLK to CSB hold time	20			ns
t_{CSB_HI}	CSB high time	10			ns

8. SPI Protocol

There are eight SPI programming modes defined by the first three mode selection bits of the SPI command word (Table 5 and Table 6). Global scope commands are interpreted by all chips on the SPI bus, regardless of the IC's hard-wired address. Local scope commands are only interpreted by ICs whose hard-wired address matches the address supplied by the SPI command word (except in the case of RF Load). Data is always loaded MSB first and latched on the rising edges of the clock.

Table 5. Read/Write Modes

Mode Selection Bits M[2:0]	Mode Description	Read/Write	Memory Location	Command Scope	SPI Command Word Length (Bits)
001	Local Register Write	Write	Static Registers	Local	40
000	Local Register Read	Read	Static Registers	Local	24
110	Local LUT Write	Write	LUT	Local	40
111	Local LUT Read	Read	LUT	Local	24
011	Global Register Write	Write	Static Registers	Global	32
010	Global LUT Write	Write	LUT	Global	32

Table 6. Fast Beam Steering Modes

Mode Selection Bits M[2:0]	Toggle Enable (TE)	Mode Description	Command Scope	SPI Command Word Length (Bits)
101	NA	Local Fast Beam Steering	Local	24
100	0	Global Fast Beam Steering without Toggle Enable	Global	16 + 8*N
100	1	Global Fast Beam Steering with Toggle Enable Global	Global	16 + 2*N

8.1 Local Register Write

The Local Register Write mode is used for configuring and controlling the chip and individual RF channel settings, including bias, gain, and phase. Only the devices matching the address supplied in the SPI command word will be written to in this mode. Continuous write is supported by appending 16-bit data sets at the end of the initial command word, with the register address automatically incremented by 1. The RF Load bits control phase and gain state latching of all chips on the SPI bus independent of their address. If RF Load is set to 01, then the data written to the CHn_SET register and the RF channels is latched into the active registers of all the devices on the bus immediately following the register write command. Otherwise, the data is written to the buffer registers and the channel state and CHn_SET registers do not get updated until the appropriate RF Load sequence is sent to any device on the SPI bus. This feature allows all the RF channel states to be updated simultaneously for all devices on the SPI bus. A write command to any register (e.g., scratch register) with RF load = 01 will trigger an update.

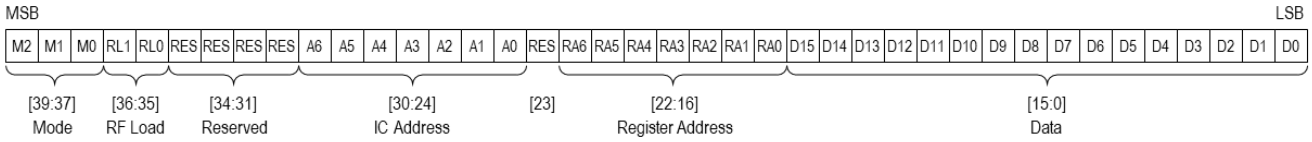


Figure 55. SPI Command Word Format for Local Register Write Mode

Table 7. Local Register Write Command Word Description

Bit Size	Field	Description	Function
[39:37]	SPI Mode	Programming mode	001 = Local register write (see Table 8)
[36:35]	RF Load	2-bit sequence to control data update to RF channels	01 = Immediate update of RF channel phase and gain state stored in CHn_SET registers.
[34:31]	Reserved Bits	Must be set to 0000	
[30:24]	Chip Address	Specifies the address of the chip to which the data will be written. Refer to the Pin Map for setting of the chip address.	Bits 28:24 correspond to the hard-wired chip address that is set by the ADD[4:0] pins. Bits 30:29 must be set to 00
23	Reserved Bit	Must be set to 0	
[22:16]	Register Address	7-bit address of register that data will be written to	
[15:0]	Data	16-bit data	This data will be written to the register specified by the Register Address field

8.2 Local Register Read

The Local Register Read mode is used for reading back the register values of the RF channel settings, including bias, gain, and phase. This mode is also used for reading temperature sensor and power detector measurements. Only the devices matching the address supplied in the SPI command word will respond in this mode. Continuous read is supported by this mode in a consecutive manner with data from the consecutive register read every 16 clock cycles until the CSB signal is set to high. After it reaches the last valid register, it rolls back to register 0.

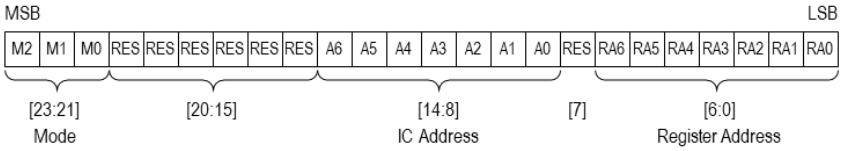


Figure 56. SPI Command Word Format for Local Register Read Mode

Table 8. Local Register Read Command Word Description

Bit Size	Field	Description	Function
[23:21]	SPI Mode	Programming mode	000 = Local register read
[20:15]	Reserved Bits	Reserved	Must be set to 000000
[14:8]	Chip Address	Specifies the address of the chip from which the data will be read. For setting of the chip address, see Pin Assignments.	Bits 12:8 correspond to the hard-wired chip address that is set by the ADD[4:0] pins (see Pin Assignments). Bits 14:13 must be set to 00.
7	Reserved Bit		Must be set to 0
[6:0]	Register Address	7-bit address of register that data will be written to	

8.3 Local LUT Write

The Local LUT Write mode is used to populate the 128 beam states for each of the 16 channels of the device. Each beam state contains 16 bits of information per channel, including the channel phase, gain, and enable states. Continuous write is supported by appending 16-bit data sets to the command word. Any data appended is first stored in the consecutive channel allocation and then the consecutive LUT address after all the channels at a particular LUT address have been written to. After the last LUT location is updated, this operation goes back to the first LUT address. RF channels and CHn_SET registers do not get automatically updated with the data that is loaded into the LUT.

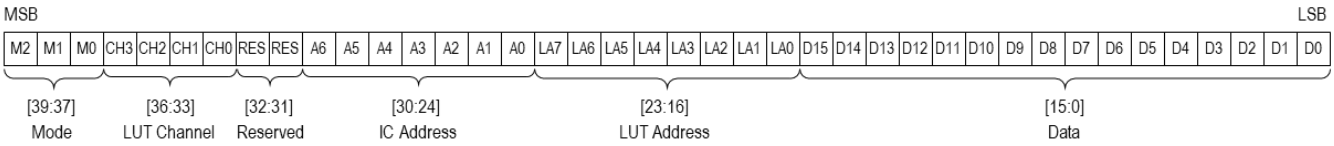


Figure 57. SPI Command Word Format for Local LUT Write Mode

Table 9. Local LUT Write Command Word Description

Bit Size	Field	Description	Function
[39:37]	SPI Mode	Programming mode	110 = Local LUT write
[36:33]	LUT Channel	Address of the channel for writing	CH[3:0] specify the LUT channel (one of 16) for writing.
[32:31]	Reserved Bits	Reserved bits	
[30:24]	Chip Address	Specifies the address of the chip to which the data will be written. Refer to the Pin Map for setting of the chip address.	Bits 28:24 correspond to the hard-wired chip address that is set by the ADD[4:0] pins (refer to Pin Map). Bits 30:29 must be set to 00
[23:16]	LUT Address	Address of the LUT entry for writing	LA[7] must be set to 0. LA[6:0] specify the LUT location (one of 128) for writing.
[15:0]	Data	16-bit data	This data is written to the LUT address location specified by LUT Channel and LUT Address.

8.4 Local LUT Read

The Local LUT Read mode is used to read back the 128 beam states for each of the 16 channels of the device. Each beam state contains 16 bits of channel phase and gain information. Continuous read is not supported at this time.

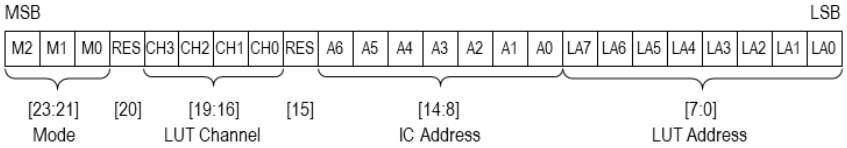


Figure 58. SPI Command Word Format for Local LUT Read Mode

Table 10. Local LUT Read Command Word Description

Bit Size	Field	Description	Function
[23:21]	SPI Mode	Programming mode	111 = Local LUT reads
20	Reserved Bit		Must be set to 0
[19:16]	LUT Channel	Address of the channel for reading	CH[3:0] specify the LUT channel (one of 16) for writing.
15	Reserved Bit		Must be set to 0
[14:8]	Chip Address	Specifies the address of the chip from which the data will be read. For setting of the chip address, see Pin Assignments.	Bits 12:8 correspond to the hard-wired chip address that is set by the ADD[4:0] pins (see Pin Assignments). Bits 14:13 must be set to 00.
[7:0]	LUT Address	8-bit address of LUT entry for reading	LA[7] must be set to 0. LA[6:0] specify the LUT location (one of 128) for reading.

8.5 Local Fast Beam Steering Mode

Local fast beam steering mode allows fast loading of any LUT entry to the RF channels for a single chip on the SPI bus. The RF channels do not get updated by the phase and gain information in the corresponding LUT address until SPI command with the correct RF Load sequence (RF Load = 01) is sent. Instead, they get stored in buffer registers until the command with the correct RL sequence is sent. All the RF channels in all the chips that are in local fast beam steering mode are updated with their buffered data when the correct RL sequence is sent regardless of the chip address information. This LUT address (which is buffered into the RF channels) information for each chip is stored in a separate register (0x03h MO_MEM_ACT) for this mode so that the user can read back that register anytime to see which LUT address is currently active on RF channels. A single reserved bit is required after 7-bit LUT address data.

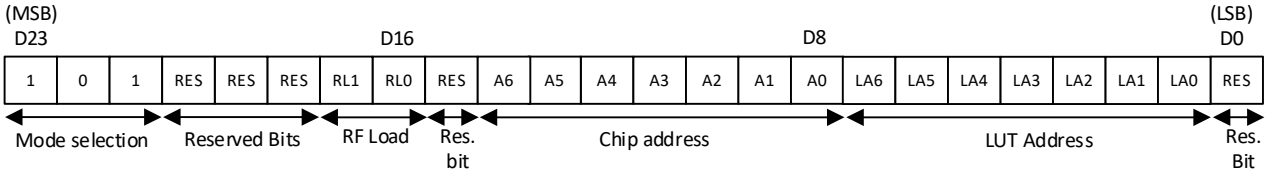


Figure 59. SPI Command Word Format for Local Fast Beam Steering Mode

Table 11. Local Fast Beam Steering Command Word Description

Bit Size	Field	Description	Function
[23:21]	SPI Mode	SPI protocol mode	101 = Local fast beam steering mode (see Table 8).
[20:18]	Reserved Bits	Must be set to 000	
[17:16]	RF Load	2-bit sequence to control data update to RF channels.	01 = Immediate update of RF channel phase, gain and power down state from LUT Address. Otherwise, data is stored in buffer registers until a command with the correct RF Load bit sequence is sent.
15	Reserved Bit	Must be set to 0	
[14:8]	Chip Address	Specifies the address of the chip to which the SPI will communicate. For setting of the chip address, see Pin Assignments.	Bits 12:8 correspond to the hardwired chip address that is set by ADD[4:0] pins. Bits 14:13 must be set to 00.
[7:1]	LUT Address	7-bit address of LUT entry to access	128 entries are available.
[0]	Reserved bit	Reserved bit	Default: 0

8.6 Global Register Write

The Global Write mode (or broadcast mode) enables simultaneous writing to all chips on the SPI bus, regardless of the chip address. Data written using this command gets loaded to the register at the corresponding register address in all the chips and RF channels are updated immediately. Continuous write is supported by this mode as long as the user keeps appending 16-bit data words at the end of the SPI command. Each 16-bit data word gets uploaded to the consecutive register starting from the register address specified by the SPI command. The global write command also supports sub-array addressing by setting the sub-array mode enable (SE) bit to 1. In this case, only the devices having sub-array address matching the SA[2:0] bits are written to. The sub-array addresses can be programmed for each device using the Local Register Write mode. Up to eight unique sub-array addresses can be defined on a given SPI bus.

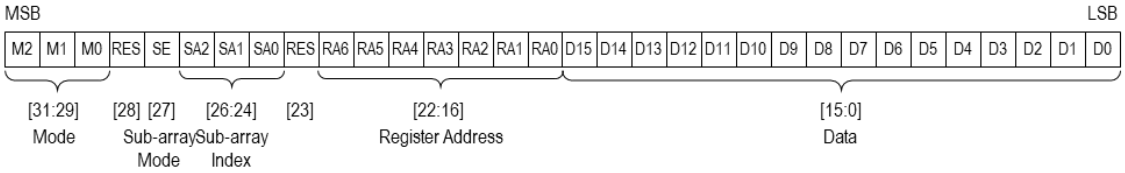


Figure 60. SPI Command Word Format for Global Register Write Mode

Table 12. Global Register Write Command Word Description

Bit Size	Field	Description	Function
[31:29]	SPI Mode	Programming mode	011 = Global Register Write Mode
[28]	Reserved Bit		Must be set to 0
[27]	Sub-array operation enable	Enables sub-array addressing	0 = Global write (all chips) 1 = Sub-array addressing enabled
[26:24]	Sub-array index	Specifies the sub-array address	Up to 8 unique values allowed
23	Reserved Bit	Must be set to 0	
[22:16]	Register Address	7-bit register address for writing	
[15:0]	Data	16-bit data	This data is written to the register location specified by the Register Address field

8.7 Global LUT Write

The Global Write mode (or broadcast mode) enables simultaneous writing to all the chips on the SPI bus, regardless of the chip address. Data sent through this command gets loaded to the LUT entry specified by LUT address and LUT channel when LUT mode bit is set to 0. If LUT mode bit is set to 1, data gets loaded to all the channel entries at the corresponding LUT address. Continuous write is supported by this mode as long as the user keeps sending 16-bit data streams at the end of the SPI word. If LUT mode is set to 0, the next set of data is loaded to the consecutive channel and after the last channel at the same LUT address, it goes on to the first channel at the consecutive LUT address. If LUT mode is set to 1, each 16-bit data gets uploaded to all the channels at the consecutive LUT address.

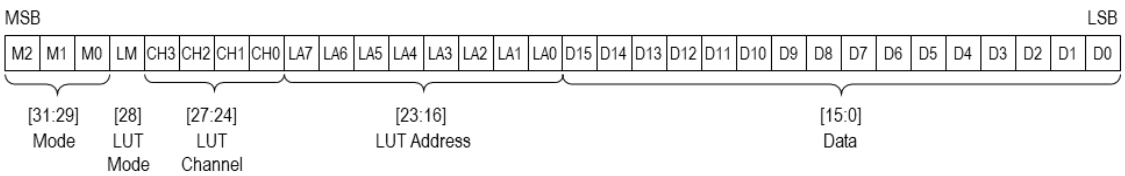


Figure 61. SPI Command Word Format for Global LUT Write Mode

Table 13. Global LUT Write Command Word Description

Bit Size	Field	Description	Function
[31:29]	SPI Mode	Programming mode	010 = Global LUT Write Mode
28	LUT write mode	Sets the LUT write mode	0 = Write to a single channel at LUT address 1 = Write to all channels at LUT address
[27:24]	LUT Channel	Address of the channel for reading	CH[3] must be set to 0. CH[2:0] specify the LUT channel (one of 16) for reading.
[23:16]	LUT Address	8-bit address of LUT entry for reading	LA[7] must be set to 0. LA[6:0] specify the LUT location (one of 128) for reading.
[15:0]	Data	16-bit data	

8.8 Global Fast Beam Steering Mode

This mode allows all channels of all devices in an array or sub-array, sharing a common SPI bus, to be updated simultaneously with gain and phase values from their respective LUTs. Continuous update is supported as long as the user keeps sending 7-bit LUT address information padded by a reserved bit at the end. This mode features sub-array functionality which is very similar to the global register write command. Sub-array function is activated by SE = 1, whereas SE = 0 indicates true global mode. Sub-array index is stored in the same register with the global register write mode. When it is activated, global fast beam steering mode command is only applied to the corresponding sub-array members.

Fast beam steering mode will also allow another optional operation scheme, which is controlled by the “toggle-enable (TE)” bit. If TE = 1, after sending the initial SPI command with 7-bit LUT address and the reserved bit, all the RF channels will be updated to the consecutive LUT beam state in every two clock cycles. If TE = 0, the user will need to keep sending 8-bit address information for continuous steering. The users will be able to switch seamlessly between the original and the optional operation scheme. For the current version, the latch of the active LUT state to RF channels happens on the rising edge of the clock. Therefore, for TE = 0 mode, if the user wants to keep a certain LUT location active for a while (not send LUT addresses one after other), there are two options: (i) send the last LUT location twice or (ii) finish up the SPI word by taking CSB high. As long as the 7-bit LUT addresses are continuous (meaning continuous beam steering), no extra action is required. For TE = 1, the latch happens on the rising edge of the clock cycle following 2 cycles indicated below. Therefore, if the user wants to stay in a certain LUT location, there are two options: (i) send an extra clock cycle after two cycles so that the latch happens (ii) finish up the SPI word by taking CSB high. If the first option is taken, it means the user needs to wait at after the 1st clock cycle after the latch label in the following figure.

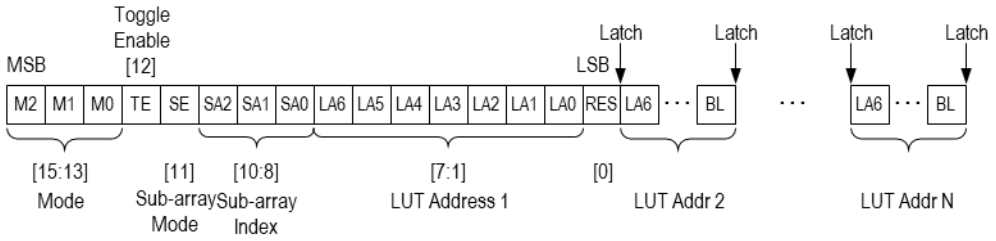


Figure 62. Global Mode Fast Beam Steering Bit Sequence TE = 0

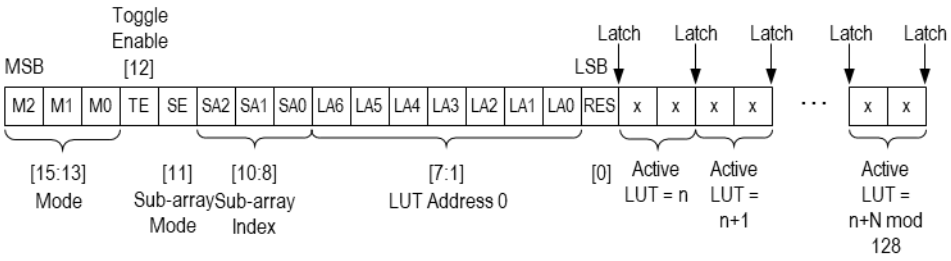


Figure 9. Global Mode Fast Beam Steering Bit Sequence TE = 1

Table 14. Global Mode Fast Beam Steering Command Bit Definitions

Bit Size	Field	Description	Function
[15:13]	SPI Mode	SPI protocol mode	100 = Global fast beam steering mode
[12]	Toggle Enable	Enables continuous beam steering	0 = Must specify 8-bit data for LUT address 1 = LUT address automatically incremented by 1, after supplying initial 8-bit LUT address
[11]	Sub-array operation enable	Enables sub-array addressing	0 = Global write (all chips) 1 = Sub-array addressing enabled
[10:8]	Sub-array index	Specifies the sub-array address	Up to 8 unique values allowed
[7:1]	LUT Address	7-bit address of LUT entry for reading	128 locations are available.
[0]	Reserved bit		Must be set to 0

9. Register Information

This section describes all of the memory registers that are accessible to the user. The hardware default (“reset”) register values are automatically set when power is first applied to the device or when the RST pin is toggled. The typical register values, when specified, were used in characterizing the typical device performance.

9.1 Register Map

Table 15. Register Map

Register Address, Hex	Register Name	Register Bit Fields	Bits	Access	Reset Value, Hex	Typical Value, Hex
00	CTRL_CFG	RESERVED	15:5	RO	0010	0000
		GLOBAL_PWD	4	RW		
		SCAN_MODE	3	WO		
		SA_Index	2:0	RW		
01	PTAT_BIAS_CFG	RESERVED	15:12	RW	0080	088A
		MB_PT2_SLOPE	11:9	RW		
		MB_PT2_EN	8	RW		
		MB_PT_ADJ	7:5	RW		
		RESERVED	4	RW		
		MB_EN	3	RW		
		RESERVED	2	RW		
		MB_BG_SEL	1	RW		
		MB_R_SEL	0	RW		
02	SCRATCH	Scratch	15:0	RW	0000	-
03	MO_MEM_ACT	Active mode	15:13	RO	0000	-
		Active LUT state	12:5	RO		
		RESERVED	4:0	RO		
05	CLK_CTRL	RESERVED	15:12	RO	0B30	0B30
		BASE_CLK_CTRL	11:8	RW		
		ADC_CLK_HIGH	7:4	RW		
		ADC_CLK_LOW	3:0	RW		

Register Address, Hex	Register Name	Register Bit Fields	Bits	Access	Reset Value, Hex	Typical Value, Hex
06	ADC_CTRL	RESERVED	15:13	RO	0000	0000
		OSC_freq	12:11	RW		
		OSC_EN	10	RW		
		TEST_MUX	9	RW		
		TEMP	8	RW		
		RESERVED	7:0	RO		
0A	ADC_TEST	RESERVED	15:2	RO	0000	0003
		CHOPPER_EN	1	RW		
		ADC_I_X2	0	RW		
0B	TEMP_DATA	RESERVED	15:11	RO	0000	-
		ADC_DONE	10	RO		
		DATA	9:0	RO		
20 **24** **28** **2C** **30** **34** **38** **3C** **40** **44** **48** **4C** **50** **54** **58** **5C**	CH1_BIAS CH2_BIAS CH3_BIAS CH4_BIAS CH5_BIAS CH6_BIAS CH7_BIAS CH8_BIAS CH9_BIAS CH10_BIAS CH11_BIAS CH12_BIAS CH13_BIAS CH14_BIAS CH15_BIAS CH16_BIAS	LNA_BIAS	15:13	RW	70DB	6EDB
		VGA_BIAS	12:9	RW		
		PS_BIAS	8:6	RW		
		ATT_BIAS	5:3	RW		
		CH_BIAS	2:0	RW		
21 **25** **29** **2D** **31** **35** **39** **3D** **41** **45** **49** **4D** **51**	CH1_CTRL CH2_CTRL CH3_CTRL CH4_CTRL CH5_CTRL CH6_CTRL CH7_CTRL CH8_CTRL CH9_CTRL CH10_CTRL CH11_CTRL CH12_CTRL CH13_CTRL	RESERVED	15:14	RW	20FF	20FF
		RESERVED	13	RW		
		ATT_BITS	12:10	RW		
		PS_PHT	9:8	RW		
		CH_MODE	7	RW		
		LNA_MODE	6	RW		
		PS_MODE	5	RW		
		ATT_MODE	4	RW		
		LNA_EN	3	RW		

Register Address, Hex	Register Name	Register Bit Fields	Bits	Access	Reset Value, Hex	Typical Value, Hex
55 **59** **5D**	CH14_CTRL CH15_CTRL CH16_CTRL	VGA_EN	2	RW		
		PS_EN	1	RW		
		ATT_EN	0	RW		
22 **26** **2A** **2E** **32** **36** **3A** **3E** **42** **46** **4A** **4E** **52** **56** **5A** **5E**	CH1_SET CH2_SET CH3_SET CH4_SET CH5_SET CH6_SET CH7_SET CH8_SET CH9_SET CH10_SET CH11_SET CH12_SET CH13_SET CH14_SET CH15_SET CH16_SET	PS_SET	15:10	RW	03F9	03F8
		VGA_SET	9:4	RW		
		LNA_SW	3	RW		
		RESERVED	2:1	RW		
		CH_PWD	0	RW		
69	LNAREF1	RESERVED	15:6	RO	0000	-
		LNA_IREF_SHUTDOWN	5	RW		
		LNA_IREF1_CONT	4:0	RW		
6A	LNAREF2	RESERVED	15:8	RO	0000	-
		LNA_IREF_MULT	7:5	RW		
		LNA_IREF2_CONT	4:0	RW		
6B **6C**	LNAREF3 LNAREF4	RESERVED	15:5	RO	0000	-
		LNA_IREFn_CONT	4:0	RW		

9.2 Register Descriptions

9.2.1. Register Name: CTRL_CFG

Address: 0x00 Reset: 0x0010 Typical: 0x0000

Table 16. Control Configuration Register (CTRL_CFG)

Bit	Field Name	Access	Reset Value	Typical Value	Description
15:5	RSV	RO	0x000	0x000	Reserved
4	GLOBAL_PWD	RW	0x01	0x00	Global channel disable. When set to 1, the local channel disable register bit CH_PWD has no effect. When set to 0, CH_PWD enables/disables individual channels.
3	SCAN_MODE	WO	0x00	-	SCAN Mode
2:0	SA_Index	RW	0x00	-	Sub-array index for the chip

9.2.2. Register Name: PTAT_BIAS_CFG

Address: 0x01 Reset: 0x0080 Typical: 0x088A

This register controls the chip master bias generator settings.

Table 17. PTAT and Bias Configuration Register (PTAT_BIAS_CFG)

Bit	Field Name	Access	Reset Value	Typical Value	Description
15:12	RSV	RW	0x00	-	Reserved
11:9	MB_PT2_SLOPE	RW	0x00	0x04	Controls the PTAT-squared slope. Only effective if MB_PT2_EN = 1.
8	MB_PT2_EN	RW	0x00	0x00	Enable PTAT-squared.
7:5	MB_PT_ADJ	RW	0x04	0x04	± 30% chip bias reference current adjustment. Channel gain changes by ~0.9dB per code step.
4	RSV	RW	0x00	0x00	Reserved
3	MB_EN	RW	0x00	0x01	Master bias generator enable
2	RSV	RW	0x00	0x00	Reserved
1	MB_BG_SEL	RW	0x00	0x01	Reserved. Must be set to 1.
0	MB_R_SEL	RW	0x00	0x00	Reserved. Must be set to 0.

9.2.3. Register Name: SCRATCH

Address: 0x02 Reset: 0x0000

This register is used as a scratch register for testing read/write or for temporary storage.

Table 18. Scratch Register (SCRATCH)

Bit	Field Name	Access	Reset Value	Typical Value	Description
15:0	Scratch	RW	0x00	-	Scratch register

9.2.4. Register Name: MO_MEM_ACT

Address: 0x03 Reset: 0x0000

Table 19. Active Mode and Memory Register (MO_MEM_ACT)

Bit	Field Name	Access	Reset Value	Typical Value	Description
15:13	Active Mode	RO	0x00	-	Returns the last programming mode used (see Table 5 and Table 6)
12:5	Active LUT State	RO	0x00	-	Returns the last LUT address that was written.
4:0	RSV	RO	0x00	-	Reserved

9.2.5. Register Name: CLK_CTRL

Address: 0x05 Reset: 0x0B30 Typical: 0x0B30

This register controls the ADC sample clock frequency and duty cycle. The ADC sample clock is derived from the on-chip 60MHz oscillator.

Table 20. Clock Control Register (CLK_CTRL)

Bit	Field Name	Access	Reset Value	Typical Value	Description
15:12	RSV	RO	0x00	-	Reserved
11:8	BASE_CLK_CTRL	RW	0x0B	0x0B	This register controls the frequency division ratio N of the ADC clock (BASE_CLK), which is derived from the on-chip 60MHz oscillator according to 60MHz/(N+1).
7:4	ADC_CLK_HIGH	RW	0x03	0x03	Select ADC clock's high width as BASE_CLK * (N + 1).
3:0	ADC_CLK_LOW	RW	0x00	0x00	Select ADC clock's low width as BASE_CLK * (N + 1).

9.2.6. Register Name: ADC_CTRL

Address: 0x06 Reset: 0x0000 Typical: 0x0000

This register is used to enable the on-chip oscillator, which in turn enables the ADC sample clock. It also triggers the ADC to digitize the analog signals from the temperature sensor and to store the results in the respective output registers.

Table 21. ADC Control Register (ADC_CTRL)

Bit	Field Name	Access	Reset Value	Typical Value	Description
15:13	RSV	RO	0x00	-	Reserved
12:11	OSC_FREQ	RW	0x00	0x00	Controls the on-chip oscillator frequency (60MHz nominal).
10	OSC_EN	RW	0x00	-	Enables the on-chip oscillator.
9	TEST_MUX	RW	0x00	-	Triggers ADC to digitize signals from the test mux (as specified by TEST_MUX register).
8	TEMP	RW	0x00	-	Triggers ADC to digitize signal from the temperature sensor.
7:0	RSV	RO	0x00	-	Reserved. Must be set to 0

9.2.7. Register Name: ADC_TEST

Address: 0x0A Reset: 0x0000

This register controls features of the on-board ADC.

Table 22. ADC Test Register (ADC_TEST)

Bit	Field Name	Access	Reset Value	Typical Value	Description
15:2	RSV	RO	0x00	0x00	Reserved
1	CHOPPER_EN	RW	0x00	0x01	Enable Chopper function. 0 = Disable inp/inm of comp swap, 1 = Enable inp/inm of comp swap periodically.
0	ADC_I_X2	RW	0x00	0x01	Double ADC current. 0 = Normal ADC current, 1 = Double ADC current

9.2.8. Register Name: TEMP_DATA

Address: 0x0B Reset: 0x0000

This register stores the digitized code value from the temperature sensor.

Table 23. Temperature ADC Data Register (TEMP_DATA)

Bit	Field Name	Access	Reset Value	Typical Value	Description
15:11	RSV	RO	0x00	-	Reserved
10	ADC_DONE	RO	0x00	-	Returns 1 when ADC data is valid, 0 otherwise.
9:0	DATA	RO	0x00	-	10-bit ADC sample data from the temperature sensor.

9.2.9. Register Name: CHn_BIAS (n = 1 - 16)

Address: 0x20, 24, 28, 2C, 30, 34, 38, 3C, 40, 44, 48, 4C, 50, 54, 58, 5C Reset: 0x70DB Typical: 6EDB

This register controls the reference current bias level of the individual components in the RF lineup of each individual channel. The overall bias level of all components in the channel is controlled with the CH_BIAS bit.

Table 24. CHn Bias Register (CHn_BIAS), n = 1 - 16

Bit	Field Name	Access	Reset Value	Typical Value	Description
15:13	LNA_BIAS	RW	0x03	0x03	LNA Bias
12:9	VGA_BIAS	RW	0x08	0x07	VGA Bias
8:6	PS_BIAS	RW	0x03	0x03	Phase shifter bias
5:3	ATT_BIAS	RW	0x03	0x03	Attenuator bias
2:0	CH_BIAS	RW	0x03	0x03	Channel bias

9.2.10. Register Name: CHn_CTRL (n = 1 - 16)

Address: 0x21, 25, 29, 2D, 31, 35, 39, 3D, 41, 45, 49, 4D, 51, 55, 59, 5D Reset: 0x20FF Typical: 0x20FF

This register allows for enabling/disabling of individual components in the RF lineup of each channel, phase, and amplitude trimming and trading channel power against performance.

Table 25. CHn Control Register (CHn_CTRL), n = 1 - 16

Bit	Field Name	Access	Reset Value	Typical Value	Description
15:14	RSV	RW	0x00	0x00	Reserved
13	RSV	RW	0x01	0x01	Reserved
12:10	ATT_BITS	RW	0x00	0x00	Attenuator trim bits.
9:8	PS_PHT	RW	0x00	0x00	Phase shifter trim bits
7	CH_MODE	RW	0x01	0x01	Bias adjustment switch for the channel
6	LNA_MODE	RW	0x01	0x01	Bias adjustment switch for the LNA
5	PS_MODE	RW	0x01	0x01	Bias adjustment switch for the phase shifter
4	ATT_MODE	RW	0x01	0x01	Bias adjustment switch for the attenuator
3	LNA_EN	RW	0x01	0x01	Enables LNA
2	VGA_EN	RW	0x01	0x01	Enables VGA
1	PS_EN	RW	0x01	0x01	Enables phase shifter
0	ATT_EN	RW	0x01	0x01	Enables attenuator

9.2.11. Register Name: CHn_SET (n = 1 - 16)

Address: 0x22, 26, 2A, 2E, 32, 36, 3A, 3E, 42, 46, 4A, 4E, 52, 56, 5A, 5E Reset: 0x03F9 Typical: 0x03F8

This register controls the enable state, phase, and gain of each channel. Phase and gain control are both monotonic with respect to the 6-bit code value of the PS_SET and VGA_SET registers, respectively. Phase increases monotonically from 0° to 360° in ~5.6° steps corresponding to PS_SET code values of 0 to 63. Gain increases monotonically with increasing values of VGA_SET. Gain adjustment has two operating ranges: a lower range controlled by VGA_SET code values 0-31 and an upper range controlled by VGA_SET code values 32-63.

Table 26. CHn Set Register (CHn_SET), n = 1 - 16

Bit	Field Name	Access	Reset Value	Typical Value	Description
15:10	PS_SET	RW	0x00	0x00	Channel phase control
9:4	VGA_SET	RW	0x3F	0x3F	Channel gain control
3	LNA_SW	RW	0x01	0x01	First amplifier stage bypass
2:1	RSV	RW	0x00	0x00	Reserved
0	CH_PWD	RW	0x01	0x00	Channel disable

9.2.12. Register Name: LNAIREFn (n = 1 - 4)

Address: 0x69, 6A, 6B, 6C Reset: 0x0000

This register controls the output current level of the current digital to analog converters (IDACs), which are used to bias external LNAs or other components.

Table 27. LNA IREF Register 1 (LNAIREF1)

Bit	Field Name	Access	Reset Value	Typical Value	Description
15:6	RSV	RO	0x00	-	Reserved
5	LNA_IREF_SHUTDOWN	RW	0x00	-	IDAC output disable. LNAIREF1 register controls all 4 outputs (n=1-4).
4:0	LNA_IREF1_CONT	RW	0x00	-	IDAC1 output current level control

Table 28. LNA IREF Register 2 (LNAIREF2)

Bit	Field Name	Access	Reset Value	Typical Value	Description
15:8	RSV	RO	0x00	-	Reserved
7:5	LNA_IREF_MULT	RW	0x00	-	IDAC output multiplier. LNAIREF2 register controls all 4 outputs (n=1-4).
4:0	LNA_IREF2_CONT	RW	0x00	-	IDAC2 output current level control

Table 29. LNA IREF Register 3-4 (LNAIREFn), n = 3,4

Bit	Field Name	Access	Reset Value	Typical Value	Description
15:5	RSV	RO	0x00	-	Reserved
4:0	LNA_IREFn_CONT	RW	0x00	-	IDACn output current level control

10. Evaluation Kit

For more information about the evaluation board, see the *F61xx Evaluation System User Guide*.

10.1 Evaluation Board Photos

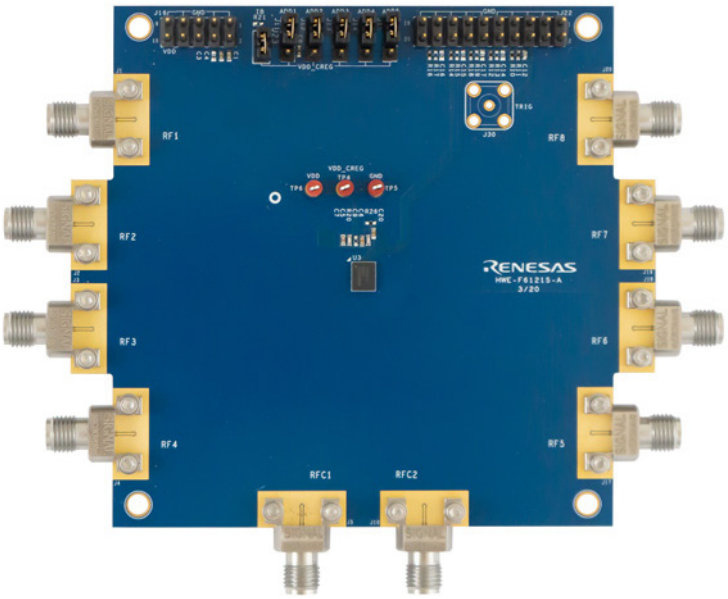


Figure 63. Evaluation Board - Top View

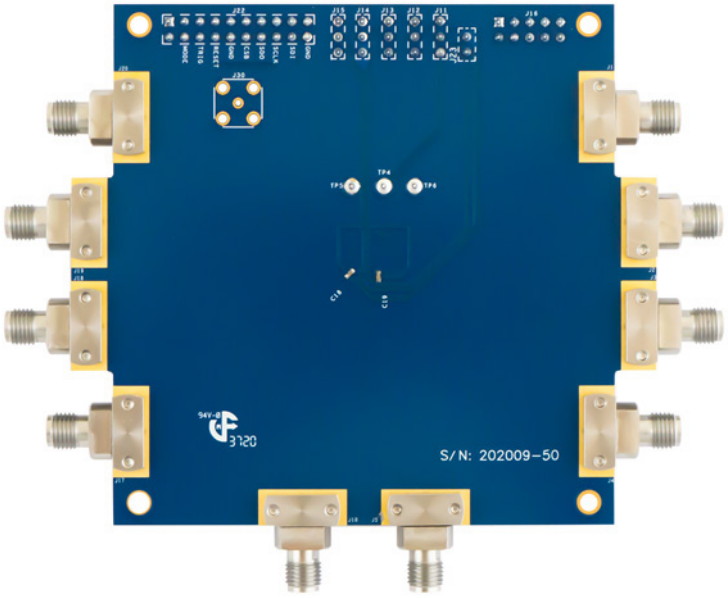


Figure 64. Evaluation Board - Bottom View

10.2 Evaluation Kit / Application Circuit

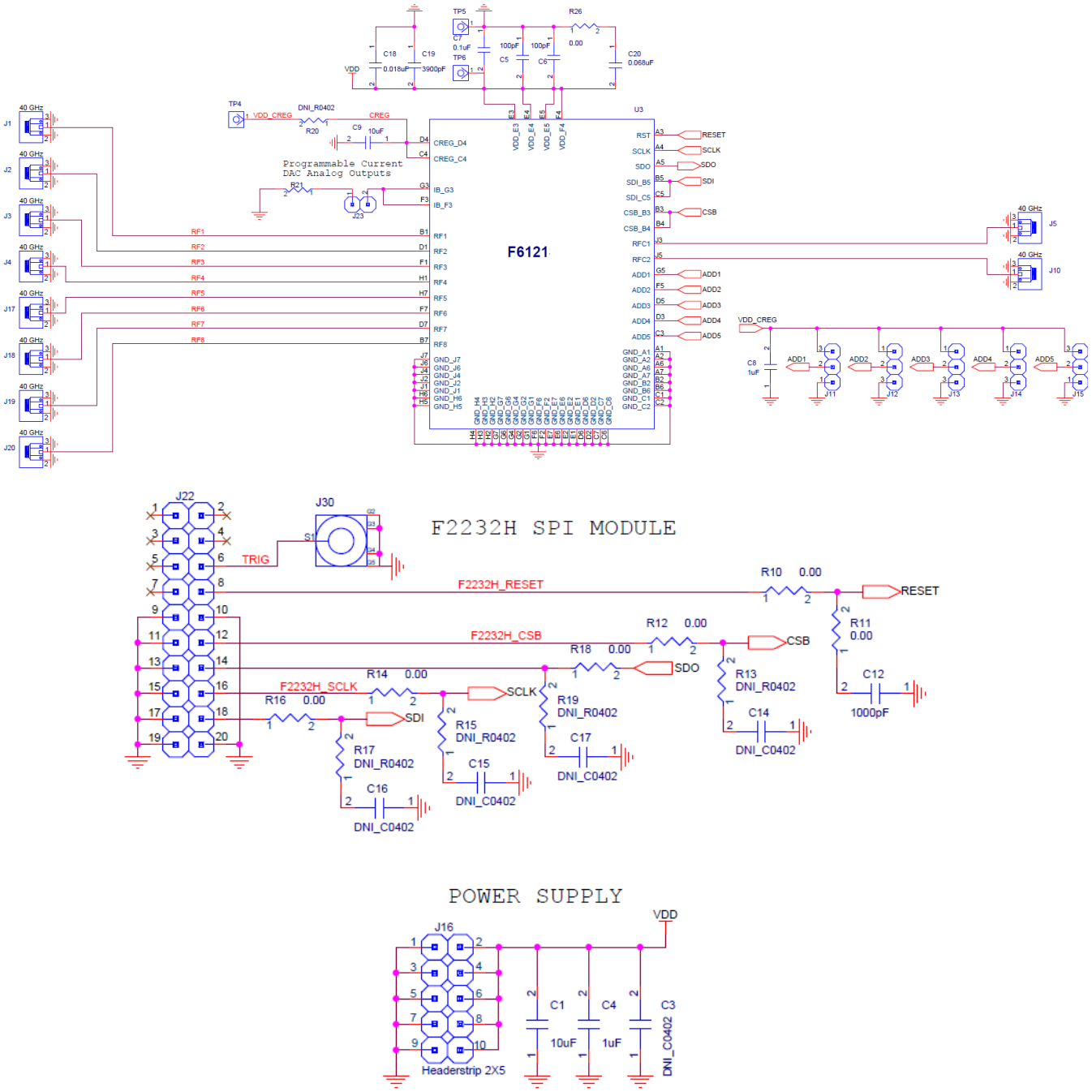


Figure 65. Evaluation Board - Schematic

Table 30. Evaluation Board Bill of Material (BOM)

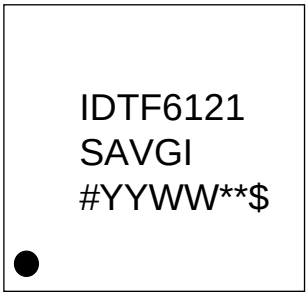
Part Reference	QTY	Description	Manufacturer Part #	Manuf.
C1	1	X5R Surface Mount Capacitor	GRM155R60J106M	
C3,C12,C14-C17	6	TBD Surface Mount Capacitor	DNI_C0402	
C4,C8	2	X5R Surface Mount Capacitor	CL05A105KA5NQNC	
C9	1	CAP CER 10UF 6.3V X6S 0402	GRM155C80J106ME11D	
C5,C6	2	COG Surface Mount Capacitor	C0402C101J3GACTU	
C7	1	X7R Surface Mount Capacitor	GRM155R71C104KA88D	
C18	1	X7R Surface Mount Capacitor	GRM155R71E183K	
C19	1	X7R Surface Mount Capacitor	GRM155R71H392J	
C20	1	X7R Surface Mount Capacitor	GRM155R71E683K	
FID1-FID3	3	Fiducial Hole	Fiducial_DNI	
J1-J5,J10,J17-J20	10	2.92mm edge launch female connector	ELF40-002	SM
J11-J15	5	Male Headerstrip, 1x3, 100mil pitch	22-28-4033	Molex
J16	1	Male Headerstrip, 2x5, 100mil pitch	10-89-7100	Molex
J30	1	Male SMB Coaxial Connector	1-1337482-0	TE
J22	1	Male Headerstrip 2x10, 100mil pitch	10-89-7200	Molex
J23	1	Male Headerstrip 1x2, 100mil pitch	10-89-4023	Molex
R11,R13,R15,R17,R19-R21	7	Surface Mount Resistor	DNI_R0402	
R10,R12,R14,R16,R18,R26	6	Surface Mount Resistor	ERJ-2GE0R00	
SO1-SO4	4	Hex Standoff Threaded M3 Nylon 0.984"	25506	Keystone
TP1,TP2,TP3,TP4,TP,TP6	6	Phosphor Bronze Wire Loop	5000	Keystone
U3	1	16-ch Dual Beam Ku Rx Beamforming IC	F6121	Renesas

11. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

12. Marking Diagram

Top view (ball side down)



- Lines 1 and 2: Renesas part number
- Line 3:
  - # is the device step
  - YYWW is the last two digits of the year and workweek code
  - **$ is the lot sequential code and mark location code

13. Ordering Information

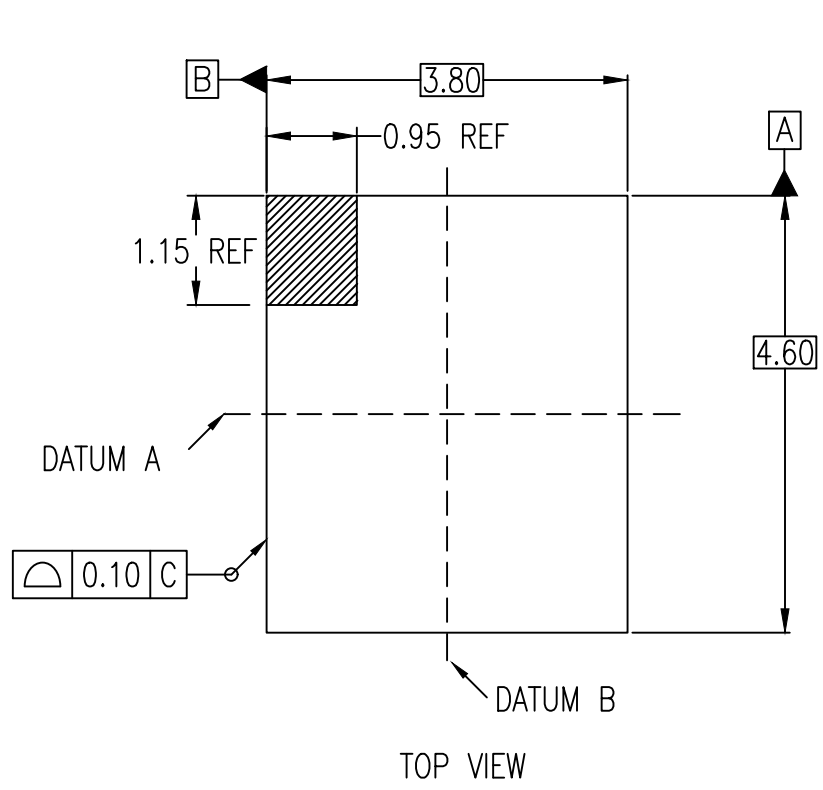
Part Number	Package	MSL Rating	Carrier Type	Temp. Range
F6121SAVGI	4.6 × 3.8 × 0.9 mm 63-FCCSP	3	Tray	-40°C to +85°C
F6121SAVGI8	4.6 × 3.8 × 0.9 mm 63-FCCSP	3	Reel	-40°C to +85°C
F6121SEVS	F6121 Evaluation System. Includes Digital Interface Board, RF Evaluation Board, USB Cable, Power Supply Cable, Digital Interconnect Cable, Evaluation Software, Device Drivers, and RF De-embed Files.			

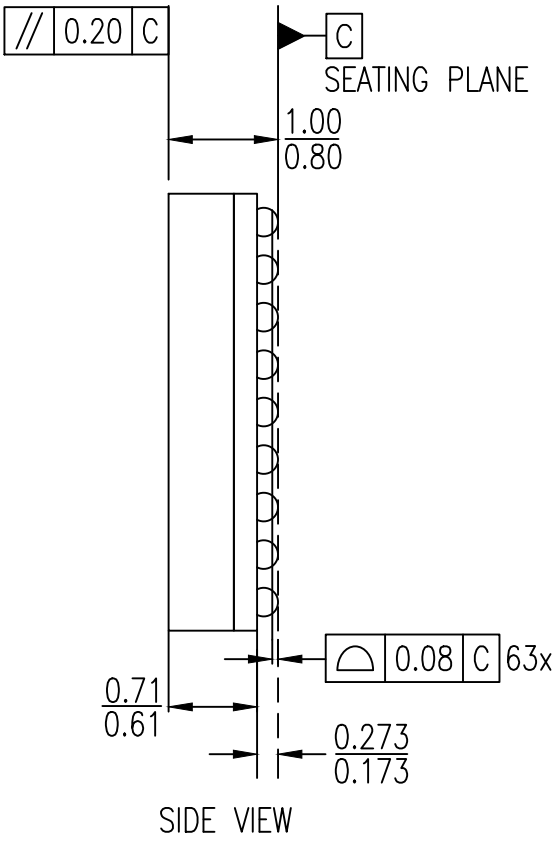
14. Revision History

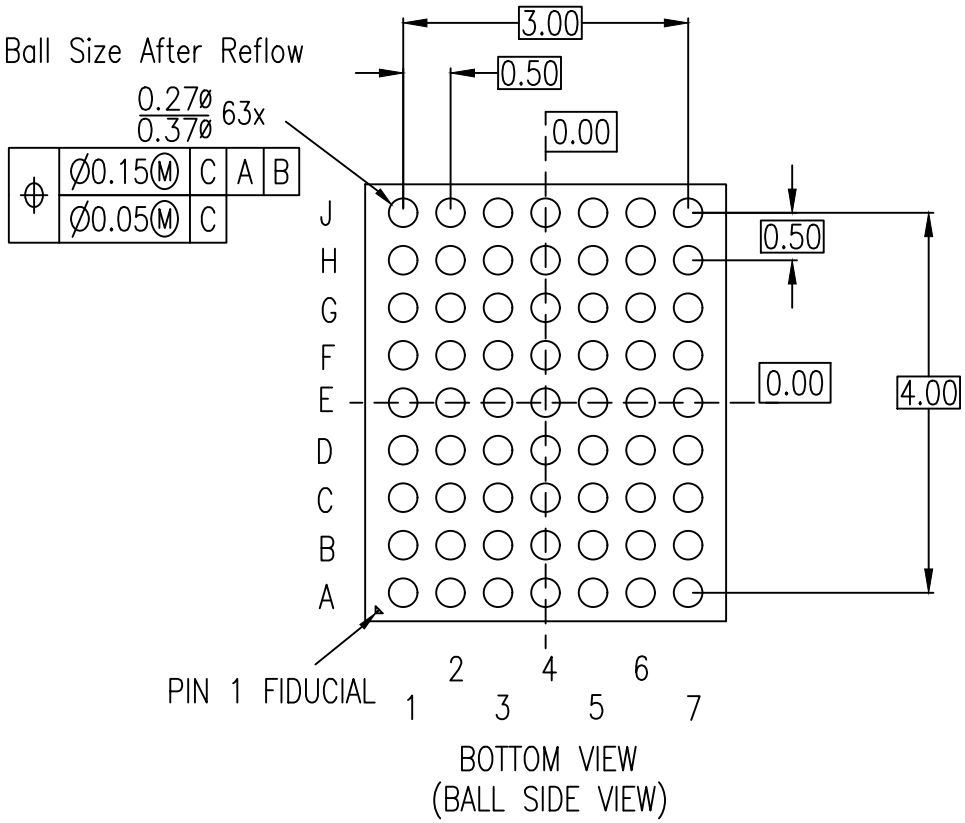
Revision	Date	Description
1.01	Dec 15, 2021	Updated the document title.
1.00	Sep 2, 2021	Initial release.

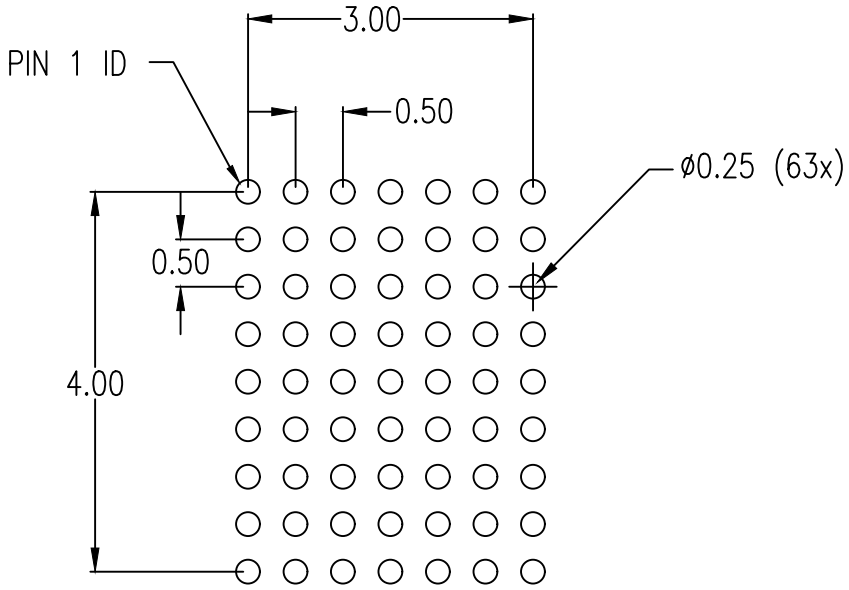
63-FCCSP, Package Outline Drawing

3.8 x 4.6 x 0.9 mm Body, 0.50mm Pitch,
AVG63D1, PSC-4817-01, Rev 00, Page 1









RECOMMENDED LAND PATTERN DIMENSION
(TOP VIEW)

NOTES:
1. ALL DIMENSION ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Revision History		
Date Created	Rev No.	Description
Nov. 5, 2019	Rev 00	Initial Release

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