SYN3339SMPLL_P22

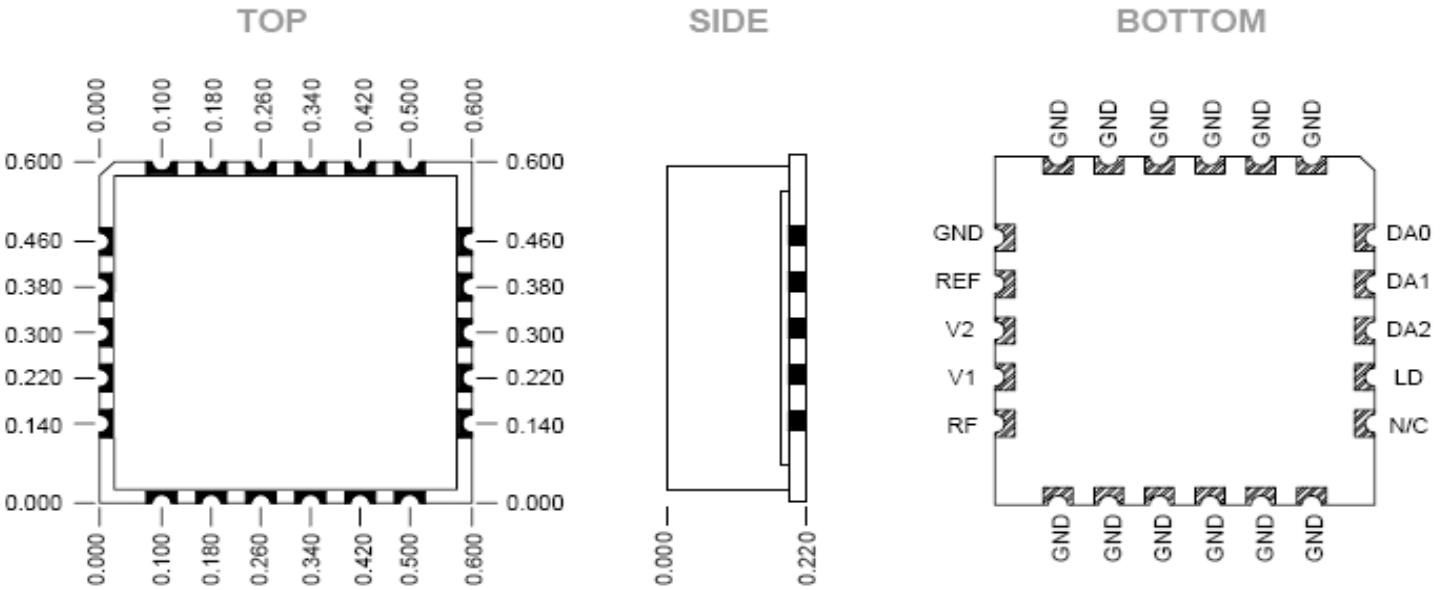
rev_0 initial rev

	MIN	TYP	MAX	UNITS	NOTES	Production Test	First Article Test
Center Frequency	3300		3899	MHz	1	..	..
Step Size		1000		KHz	1	..	..
Loop Filter		Internal					
Lock Time (within 1KHz)			25	msec	3	..	..
Reference Frequency (external)		10		MHz		..	..
Reference Amplitude	0		3.3	Vp-p			
Output Power (sinewave)	-4	0	4	dBm	1	..	..
Output Impedance		50		ohms	2		
Phase Noise @							
1 KHz Offset		-88	-83	dBc/Hz	1	..	..
10 KHz Offset		-88	-83	dBc/Hz	1	..	..
100 KHz Offset		-112	-107	dBc/Hz	1	..	..
1MHz Offset		-132	-127	dBc/Hz	1	..	..
Spurious		-70	-60	dBc	3	..	..
Reference Feedthrough		-75	-65	dBc	3	..	..
Harmonics		-15	-10	dBc	3	..	..
V1		12.5		V	1	..	..
I1		50	60	mA	1	..	..
V2	2.70	3.0	3.30	V	1	..	..
I2		25	35	mA	1	..	..
Operating Temperature	-40		+85	C	3	..	..
Package							
Length		0.600		inch	5	..	..
Width		0.600		inch	5	..	..
Height		0.22		inch	5	..	..
Programming		SPI					
PLL		Compliant with PNP Product LIne			8		
LD (Locked/Not Locked)		Locked = High			9	..	..

Notes

1. Tested in production, and guaranteed
2. Per current design, not a tested parameter
3. Sample tested from production lot and guaranteed
4. Not a tested or guaranteed design goal
5. By inspection
6. Design goal subject to change
7. Reference dependent
8. ADF4106, SPI & LD Level = +3.0V
9. This is the MUX output port; can be re-assigned via software

PACKAGE AND PIN DESCRIPTIONS



RF	RF Output. AC coupled
V1	Vcc for VCO and related circuitry. Vcc noise should be 22nV/Hz or less.
V2	Vcc for PLL and related circuitry. Vcc noise should be 22nV/Hz or less
REF	Reference Input. This port is cap coupled and is high impedance.
DA0	This is the programming LE input
DA1	This is the programming DATA input
DA2	This is the programming CLK input
LD	Lock Detect. Active High indicates a locked state. Can be re-programmed for additional functions.
GND	Analog and RF ground.