CMX90A002 1 W – 2 W 860 – 960 MHz Power Amplifier

Description

The CMX90A002 is a two-stage, fully matched MMIC PA delivering +32.5 dBm of saturated output power for use in the 860 – 960 MHz frequency range, applicable to license-free bands.

The CMX90A002 is optimised for maximum efficiency at a wide-range of collector voltages of 1.9 – 4.5 V, making it suitable for systems operating either from a Supercapacitor backup storage, or from a single-cell Li-Ion battery.

The CMX90A002 is highly integrated for ease of use, minimising external component count and reducing board area. RF input and output matching are incorporated on-chip, as well as active bias circuitry and input DC-blocking capacitor.

Using advanced GaAs HBT technology to provide a combination of high efficiency and gain, the CMX90A002 is intended as both a booster PA for the sub-1GHz band in low-voltage systems, and a high-power final stage ISM band PA in wireless applications for higher-voltage use.

The CMX90A002 is packaged in a small 3 mm x 3 mm VQFN plastic package; ideal for systems where board-space is limited.

Applications

- Automatic meter readers (AMR)
- Smart meters
- Wireless modules
- Final stage PA
- Internet of Things (IoT)
- 868 / 915 MHz ISM
- Li-Ion battery powered systems

Ordering Information

Part Number	Description
CMX90A002QF-R710	7” Reel with 1,000 pieces
CMX90A002QF-R350	13” Reel with 5,000 pieces
EV90A002	Evaluation board

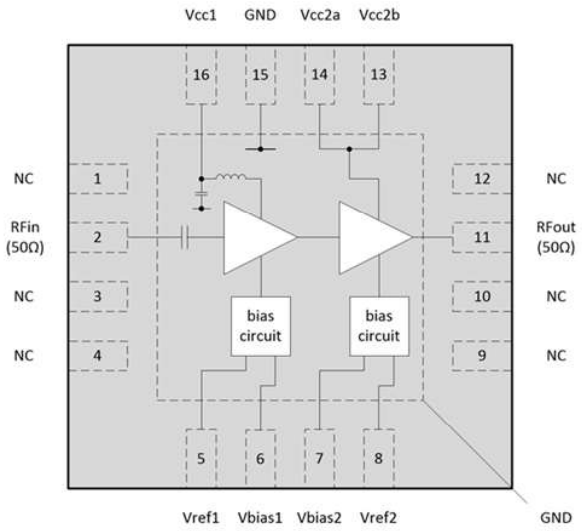


3 x 3 mm VQFN-16 Package

Product Features

- Frequency range 860 – 960 MHz
- Supply voltage 1.9 – 4.5 V
- Output power: 32.5 dBm @ 3.6 V
  29.5 dBm @ 2.5 V
- Input and output matched to 50 Ω
- Small signal gain 30 dB
- High PAE 49 %
- Shut-down and output power control

Block Diagram



Absolute Maximum Ratings

Parameter	Rating
RF Input Power	+13 dBm
Device Voltage (Vcc1, Vcc2)	+5 V
Pdiss	2.68 W @ Tc = +85 °C
Case Temperature (Tc)	-40 to +85 °C
Junction Temperature (Tjmax)	+160 °C (MTTF = 10^6 hours)
Storage Temperature	-40 to +125 °C
ESD Sensitivity	HBM 250 V (Class 1A); CDM 250 V (Class C1)
MSL Level	Level 3

Exceeding the maximum ratings may result in damage or reduced device reliability.

Thermal Characteristics

Parameter	Rating
Thermal Resistance (Rjc)	28 °C / W

Thermal resistance is junction-to-case, where case refers to the exposed die pad on the backside which is in contact with the board.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Operating Frequency Range	860		960	MHz
Quiescent Current (Icq)		75		mA
Case Temperature (Tc)	-40		+85	°C
Device Voltage (Vcc1, Vcc2)	1.9	3.6	4.5	V
Bias Voltage (Vbias1, Vbias2)	1.9	3.3	4.5	V
Current into Vref1		2.78	5	mA
Current into Vref2		2.88	5	mA

The device will be tested under certain conditions, but performance is not guaranteed over the full range of recommended operating conditions.

ESD Caution



High-performance RF integrated circuits are highly sensitive to electrostatic discharge (ESD) and may contain unprotected inputs and outputs. Handling and assembly should be conducted in an ESD-controlled environment. It is recommended that ESD precautions and protocols are adopted to minimise the risk of electrostatic discharge and protect product integrity.

Electrical Specification

Measured result on the EV90A002 EVB will include losses in the PCB tracking and DC blocking capacitor (typically 0.2 dB output loss from device to output connector).

Vcc = +2.5 V

Zo = 50 Ω, Vcc = +2.5 V, Vbias = +3.3 V, Vref = +3.3 V, Pin = +5 dBm, Ta = +25 °C (unless otherwise noted)

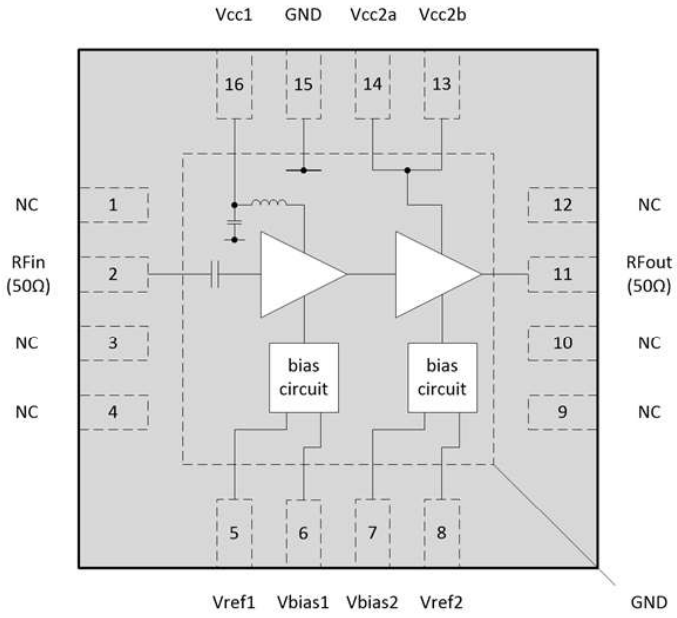
Parameter	Conditions	Min	Typ	Max	Units
Frequency		860		960	MHz
Psat	915 MHz		29		dBm
Small Signal Gain	915 MHz, Pin = -20 dBm		30		dB
PAE	915 MHz		49		%
Current Consumption (Icc)	915 MHz		0.7		A
Input Return Loss	Pin = -20 dBm		-12		dB
Output Return Loss	Pin = -20 dBm		-7		dB
2Fo	At Psat		-26		dBc
3Fo	At Psat		-48		dBc
Quiescent Current (Icq)	RF off		70		mA
Standby Current	Vcc current in standby mode, RF off		5		uA
Vbias1, 2	Supply voltage for active bias circuitry		3.3		V
Vbias Current	Vbias 1 & 2 total current. RFin = +5 dBm		8		mA
Vctrl1, 2	Vref pins require external 270R series resistors		3.3		V
Vctrl1, 2 (Standby)	PA placed into standby mode	0		1.5	V
Vctrl Current	Vctrl 1 & 2 total current. RFin = +5 dBm		5.6		mA
Output Power Control	Vref can be used to ramp between min and max output power.		70		dB
Turn-On Time	Vref = 0 V to 3.3 V		TBD		ns
Turn-Off Time	Vref = 3.3 V to 0 V		TBD		ns

Vcc = +3.6 V

Zo = 50 Ω, Vcc = +3.6 V, Vbias = +3.3 V, Vref = +3.3 V, Pin = +5 dBm, Ta = +25 °C (unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
Frequency		860		960	MHz
Psat	915 MHz		32.5		dBm
Small Signal Gain	915 MHz, Pin = -20 dBm		31		dB
PAE	915 MHz		49		%
Current Consumption (Icc)	915 MHz		1.0		A
Input Return Loss	Pin = -20 dBm		-12		dB
Output Return Loss	Pin = -20 dBm		-7		dB
2Fo	At Psat		-26		dBc
3Fo	At Psat		-48		dBc
Output Load VSWR, Ruggedness	At 915 MHz, all phase angles, Vcc = Vbias = 4.0 V. No damage	10:1			
	At 915 MHz, all phase angles, Vcc = Vbias = 4.5 V. No damage	5:1			
Output Load VSWR, Stability	At 915 MHz, all phase angles, Vcc = Vbias = 4.0 V, Spurious <-36 dBm	5:1			
Quiescent Current (Icq)	RF off		75		mA
Standby Current	Vcc current in standby mode, RF off		5		uA
Vbias1, 2	Supply voltage for active bias circuitry		3.3		V
Vbias Current	Vbias 1 & 2 total current. RFin = +5 dBm		12		mA
Vctrl1, 2	Vref pins require external 270R series resistors		3.3		V
Vctrl1, 2 (Standby)	PA placed into standby mode	0		1.5	V
Vctrl Current	Vctrl 1 & 2 total current. RFin = +5 dBm		5.66		mA
Output Power Control	Vref can be used to ramp between min and max output power.		70		dB
Turn-On Time	Vref = 0 V to 3.3 V		TBD		ns
Turn-Off Time	Vref = 3.3 V to 0 V		TBD		ns

Pin Assignments



Top View

Pin	Name	Description
1	NC	Connect to GND
2	RFin	RF input. Internally matched to 50 Ω with integrated DC-blocking capacitor.
3	NC	Connect to GND
4	NC	Connect to GND
5	Vref1	Sets bias current to driver stage. Regulated voltage and external series resistor required. Also used for on/off and power control.
6	Vbias1	Supplies base current to driver stage
7	Vbias2	Supplies base current to final stage
8	Vref2	Sets bias current to final stage. Regulated voltage and external series resistor required. Also used for on/off and power control.
9	NC	Connect to GND
10	NC	Connect to GND
11	RFout	RF output. Internally matched to 50 Ω. External DC-blocking capacitor required.
12	NC	Connect to GND
13	Vcc2b	Collector supply to final stage
14	Vcc2a	Collector supply to final stage
15	GND	Connect to GND
16	Vcc1	Collector supply to driver stage with integrated RF choke
Die pad	GND	DC and RF ground. Exposed die pad must be connected to GND.

Notes

CML recommends that all no connect (NC) pins are connected to ground.

The bottom exposed die pad must be connected to the ground plane on the board, note guidance given in the application information section.

Typical Performance

The following plots show typical performance characteristics of CMX90A002 measured on the evaluation board (Part Number EV90A002). The measurements include input and output circuit losses associated with the evaluation board.

Results are shown for two supply voltages; Vcc = +2.5 V (nominally Psat ~29.5 dBm), and Vcc = +3.6 V (nominally Psat ~32.5 dBm).

Vcc = +2.5 V

Test conditions unless otherwise noted:-

Vcc = +2.5 V, Vbias = Vctrl = +3.3 V, Ta = +25 °C, Zo = 50 Ω

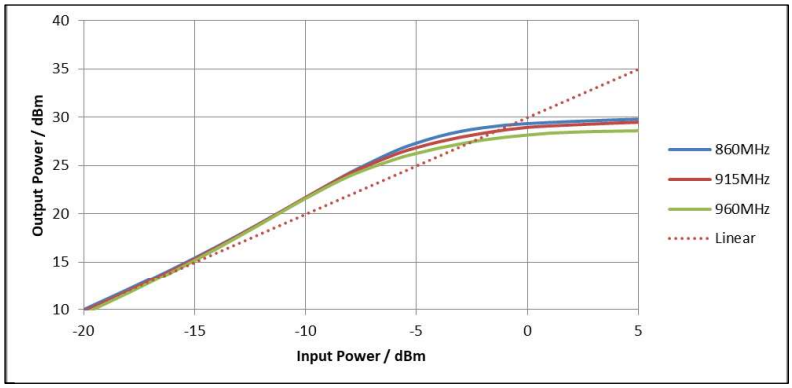


Figure 1 - Output Power v Input Power

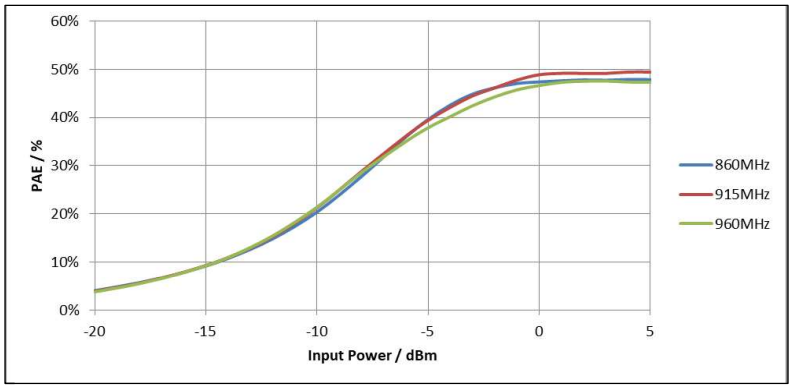


Figure 2 - PAE v Input Power

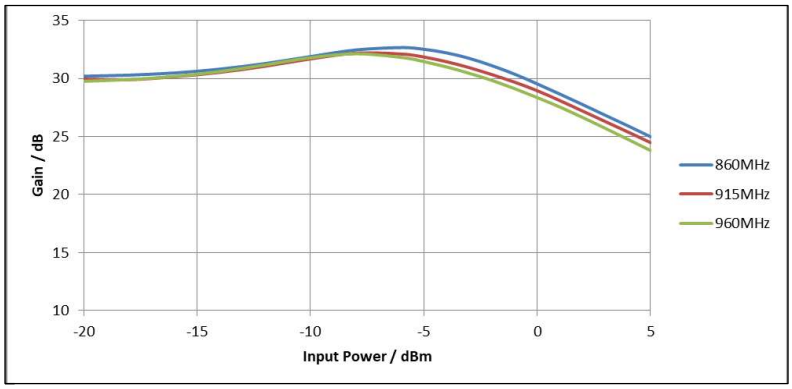


Figure 3 - Gain v Input Power

Test conditions unless otherwise noted:-

Vcc = 2.5 V, Vbias = Vctrl = 3.3 V, Ta = +25 °C, Zo = 50 Ω

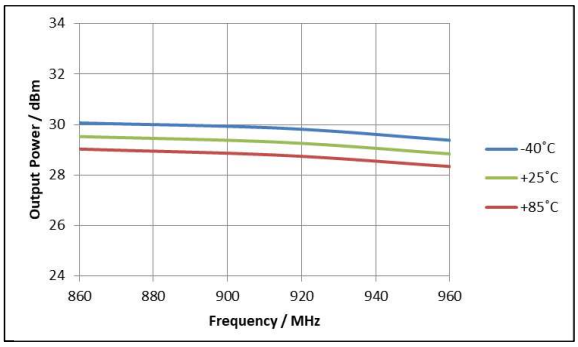


Figure 4 - Output Power (+2 dBm Pin)

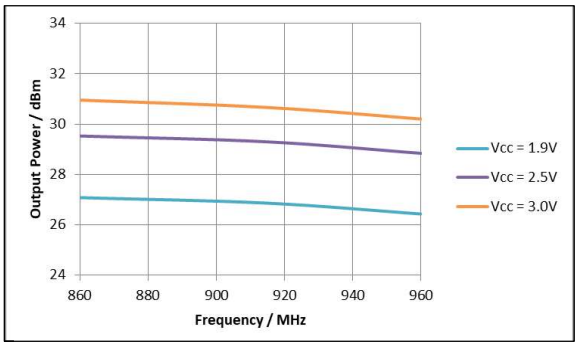


Figure 5 - Output Power (+2 dBm Pin)

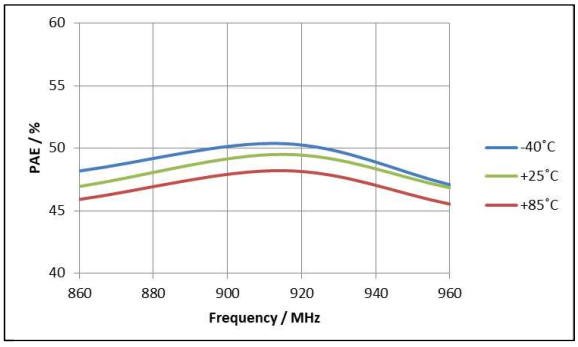


Figure 6 - PAE (+2 dBm Pin)

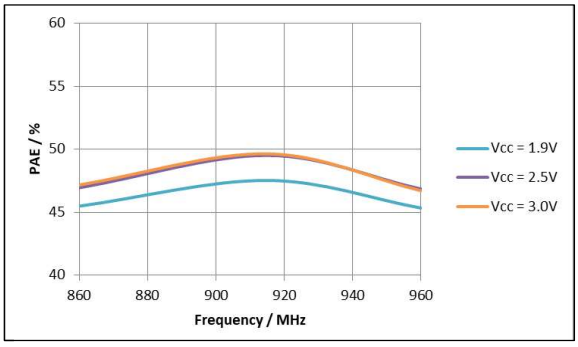


Figure 7 - PAE (+2 dBm Pin)

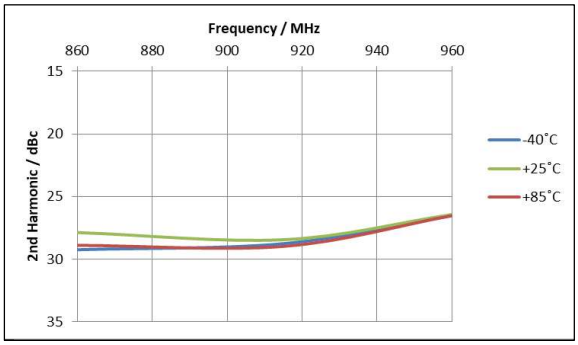


Figure 8 - 2nd Harmonic (+2 dBm Pin)

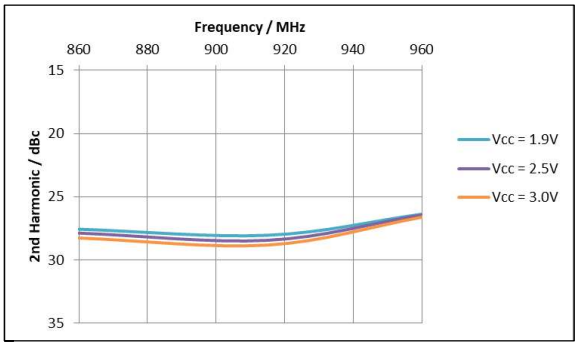


Figure 9 - 2nd Harmonic (+2 dBm Pin)

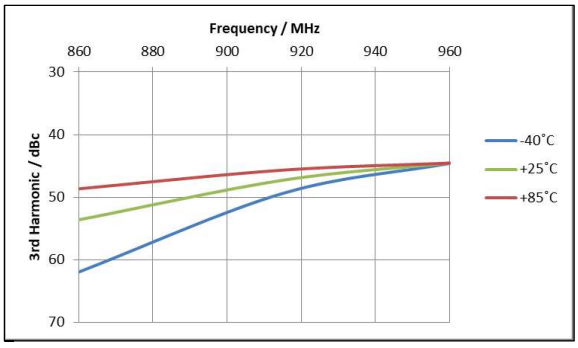


Figure 10 - 3rd Harmonic (+2 dBm Pin)

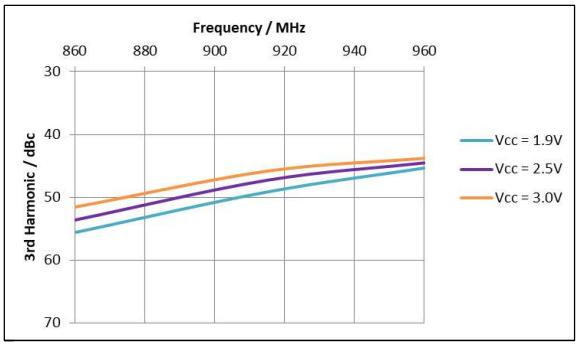


Figure 11 - 3rd Harmonic (+2 dBm Pin)

Test conditions unless otherwise noted:-

Vcc = 2.5 V, Vbias = Vctrl = 3.3 V, Ta = +25 °C, Zo = 50 Ω

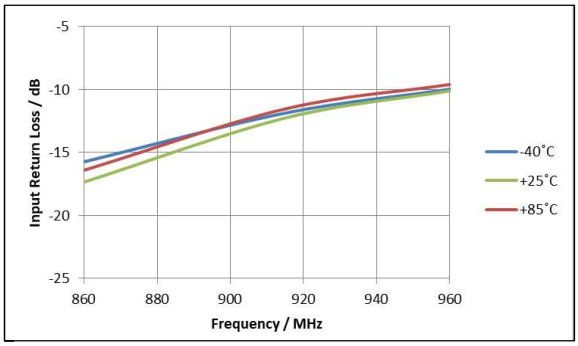


Figure 12 - Input Return Loss (+2 dBm Pin)

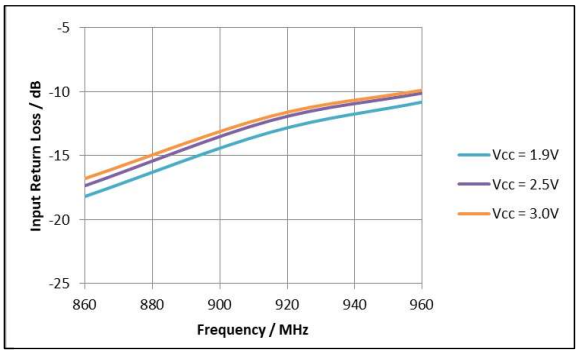


Figure 13 - Input Return Loss (+2 dBm Pin)

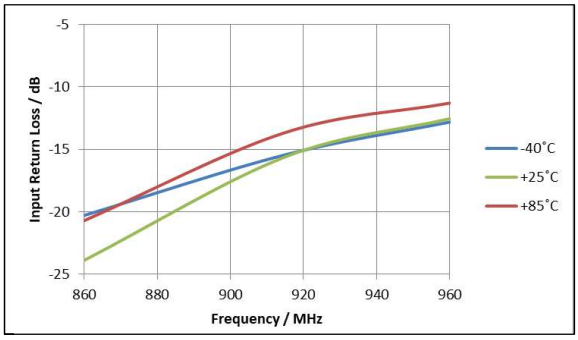


Figure 14 - Input Return Loss (-20 dBm Pin)

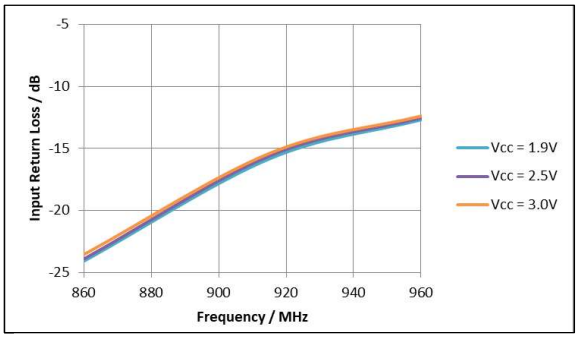


Figure 15 - Input Return Loss (-20 dBm Pin)

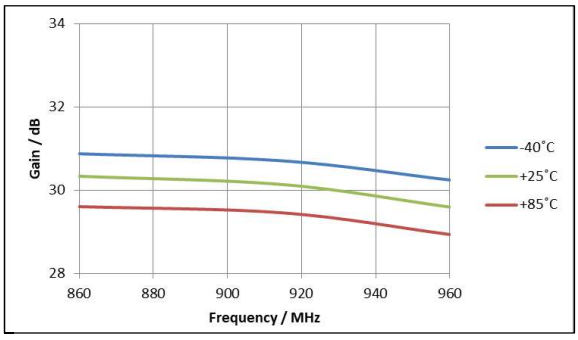


Figure 16 - Gain (-20 dBm Pin)

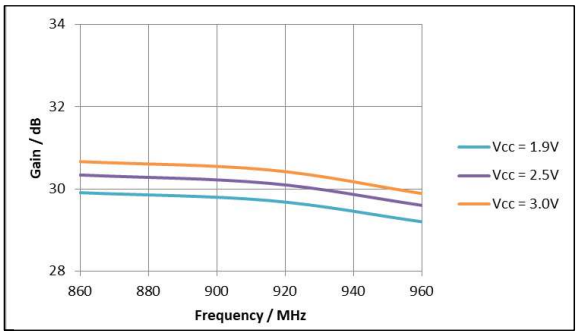


Figure 17 - Gain (-20 dBm Pin)

Test conditions unless otherwise noted:-

Vcc = 2.5 V, Vbias = Vctrl = 3.3 V, Ta = +25 °C, Zo = 50 Ω

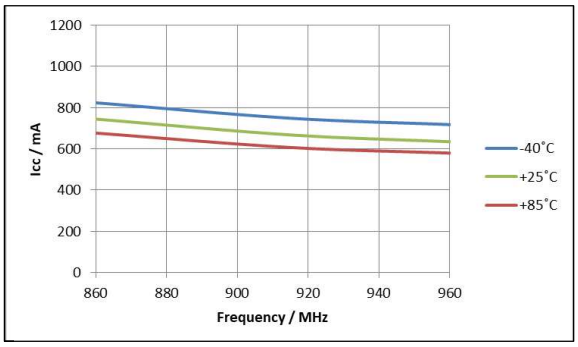


Figure 18 - Icc (+2 dBm Pin)

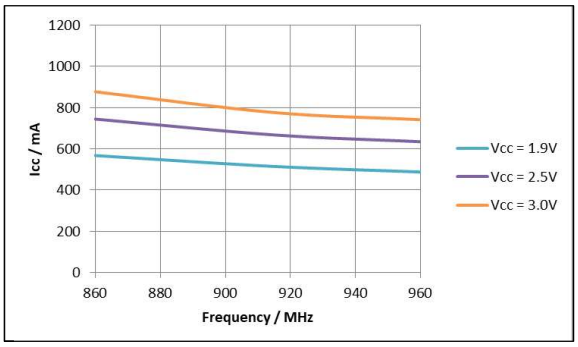


Figure 19 - Icc (+2 dBm Pin)

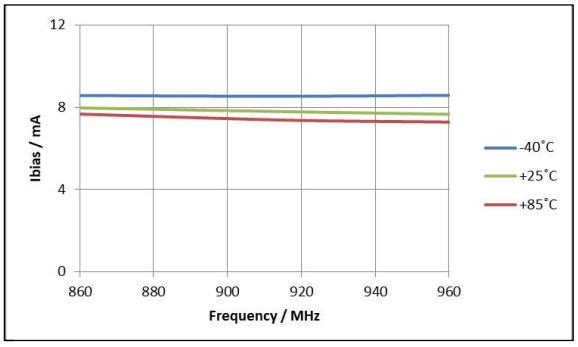


Figure 20 - Ibias (+2 dBm Pin)

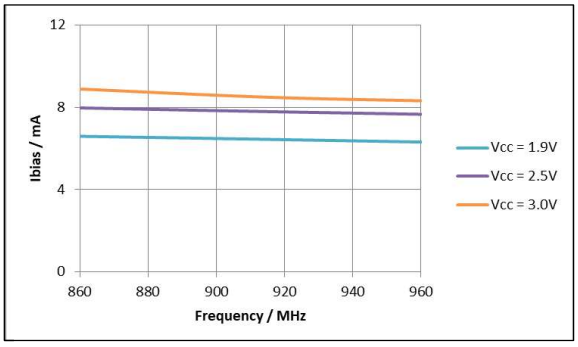


Figure 21 - Ibias (+2 dBm Pin)

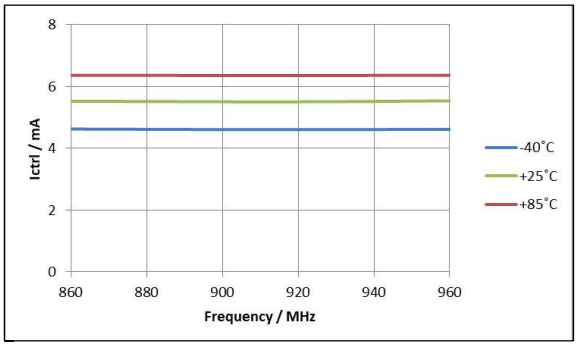


Figure 22 - Ictrl (+2 dBm Pin)

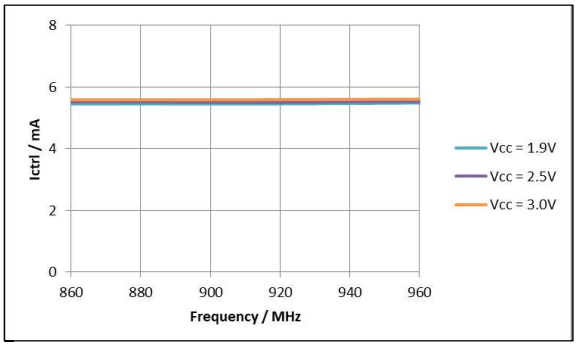


Figure 23 - Ictrl (+2 dBm Pin)

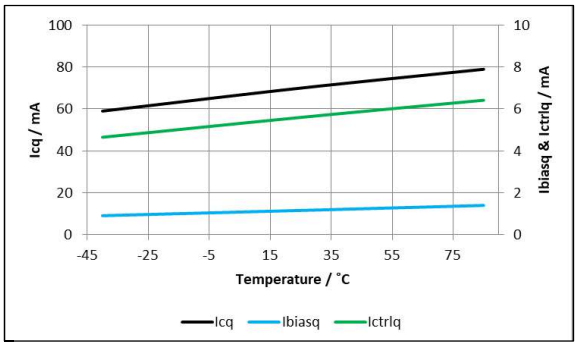


Figure 24 - Quiescent Currents

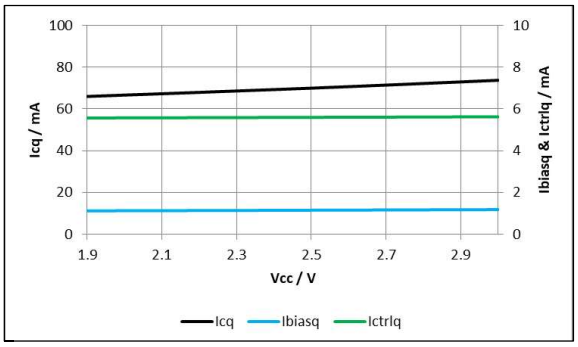


Figure 25 - Quiescent Currents

Test conditions unless otherwise noted:-

Vcc = 2.5 V, Vbias = Vctrl = 3.3 V, Ta = +25 °C, Zo = 50 Ω, Pin = -20 dBm

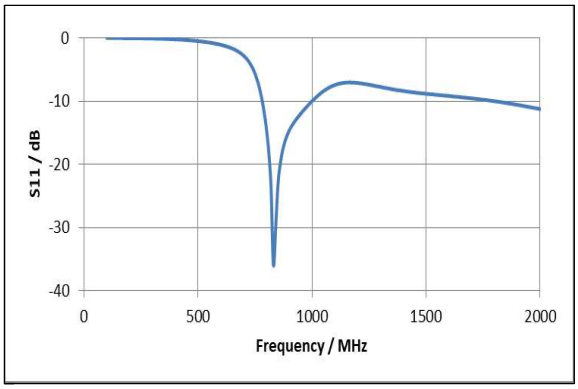


Figure 26 - Input Return Loss (S11)

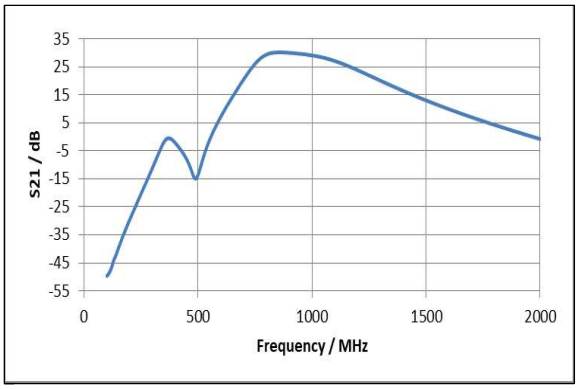


Figure 27 - Small Signal Gain (S21)

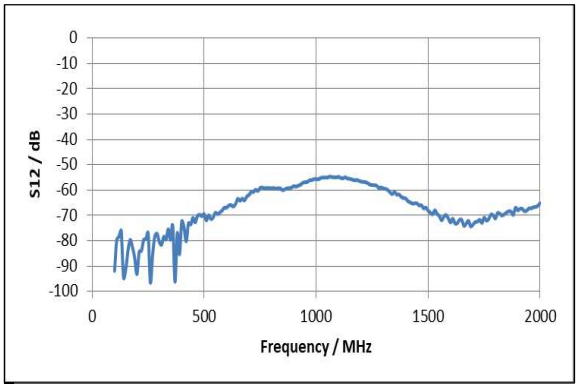


Figure 28 - Reverse Isolation (S12)

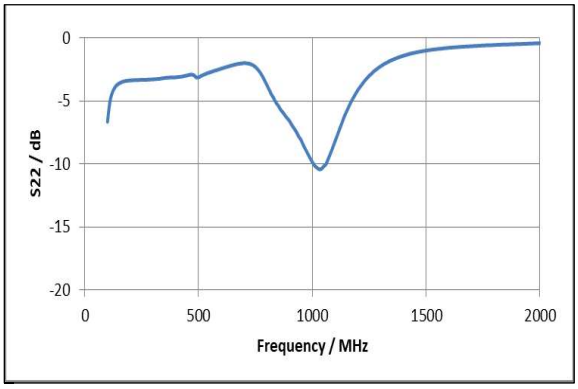


Figure 29 - Output Return Loss (S22)

Vcc = +3.6 V

Test conditions unless otherwise noted:-

Vcc = +3.6 V, Vbias = Vctrl = +3.3 V, Ta = +25 °C, Zo = 50 Ω

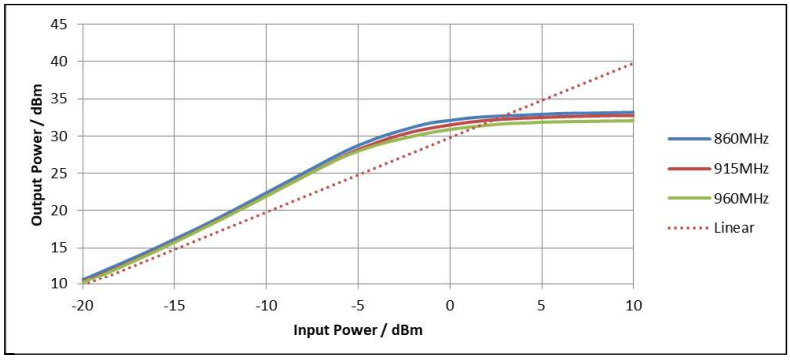


Figure 30 - Output Power v Input Power

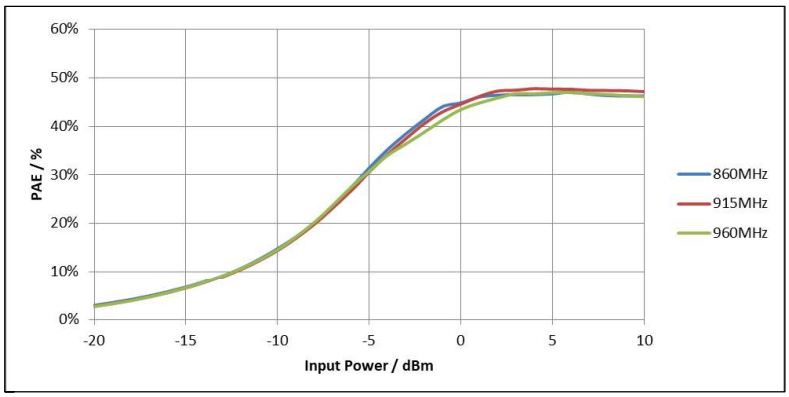


Figure 31 - PAE v Input Power

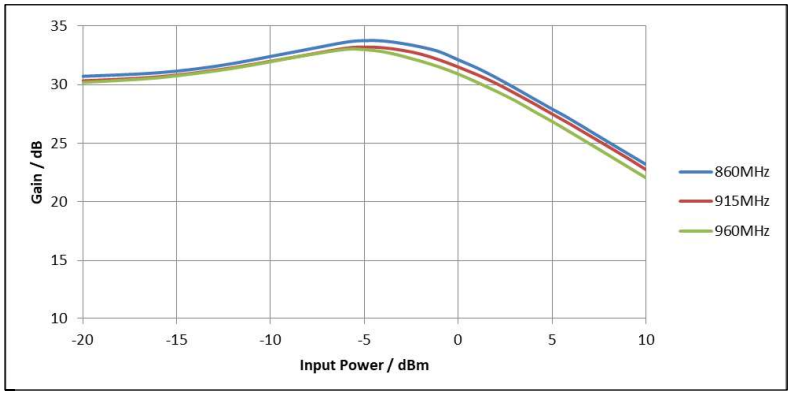


Figure 32 - Gain v Input Power

Test conditions unless otherwise noted:-

Vcc = 3.6 V, Vbias = Vctrl = 3.3 V, Ta = 25 °C, Zo = 50 Ω

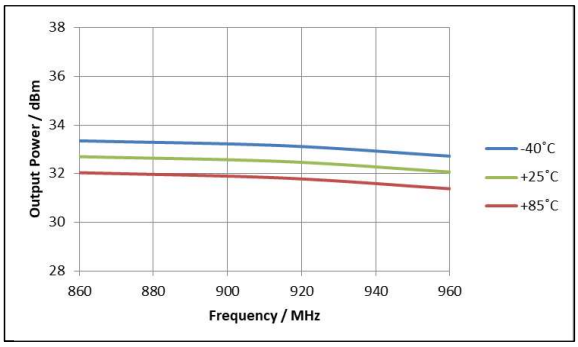


Figure 33 - Output Power (+5 dBm Pin)

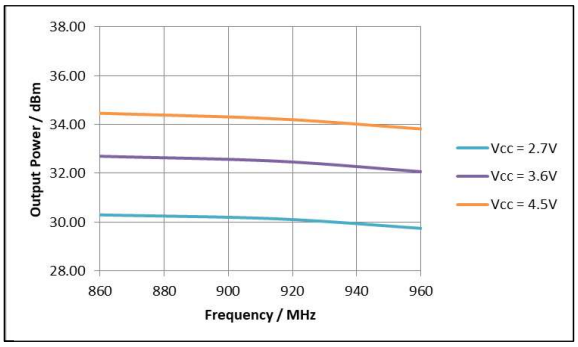


Figure 34 - Output Power (+5 dBm Pin)

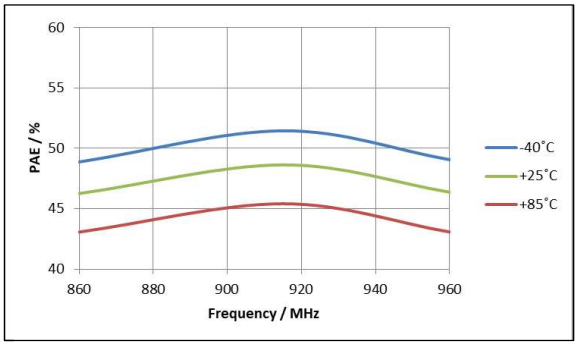


Figure 35 - PAE (+5 dBm Pin)

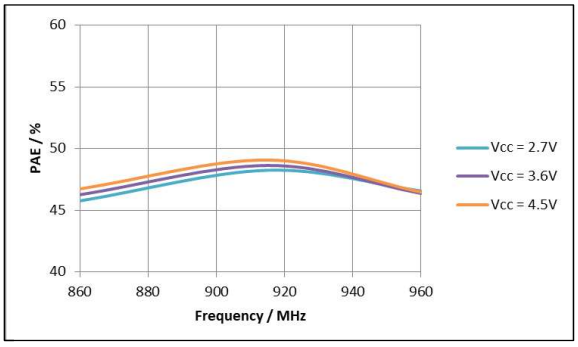


Figure 36 - PAE (+5 dBm Pin)

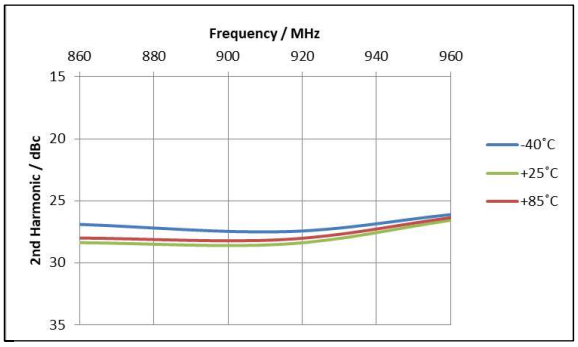


Figure 37 - 2nd Harmonic (+5 dBm Pin)

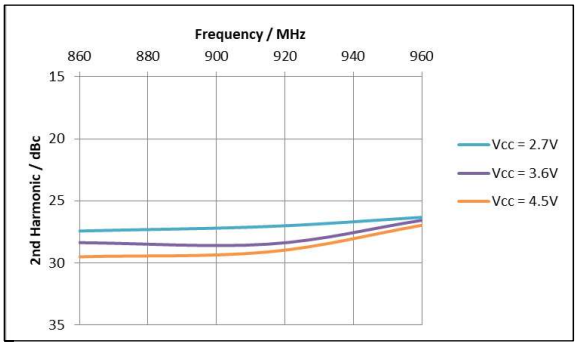


Figure 38 - 2nd Harmonic (+5 dBm Pin)

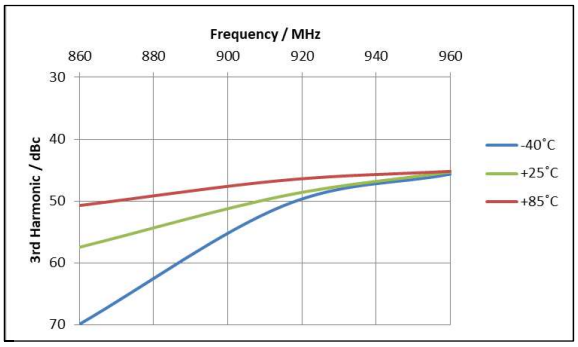


Figure 39 - 3rd Harmonic (+5 dBm Pin)

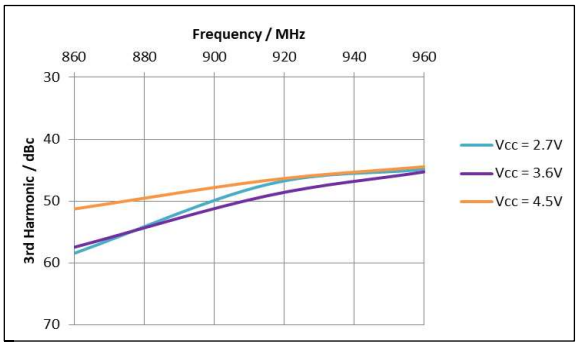


Figure 40 - 3rd Harmonic (+5 dBm Pin)

Test conditions unless otherwise noted:-

Vcc = 3.6 V, Vbias = Vctrl = 3.3 V, Ta = 25 °C, Zo = 50 Ω

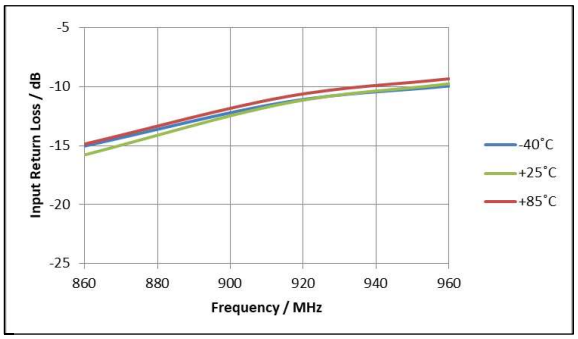


Figure 41 - Input Return Loss (+5 dBm Pin)

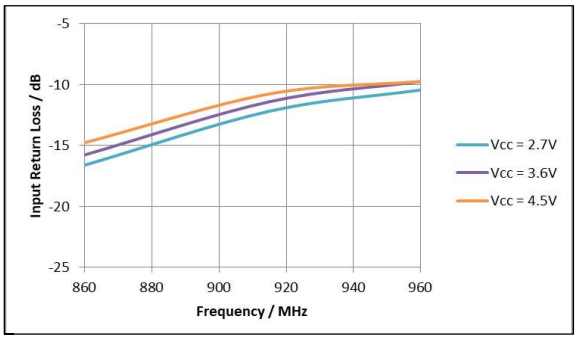


Figure 42 - Input Return Loss (+5 dBm Pin)

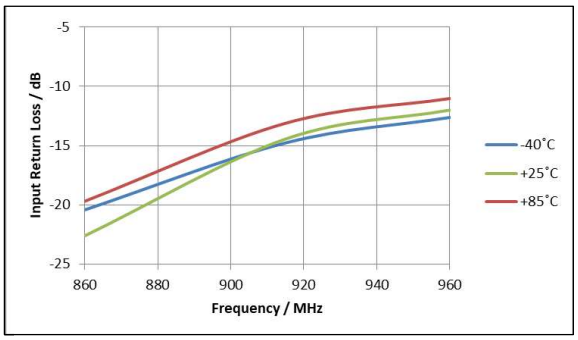


Figure 43 - Input Return Loss (-20 dBm Pin)

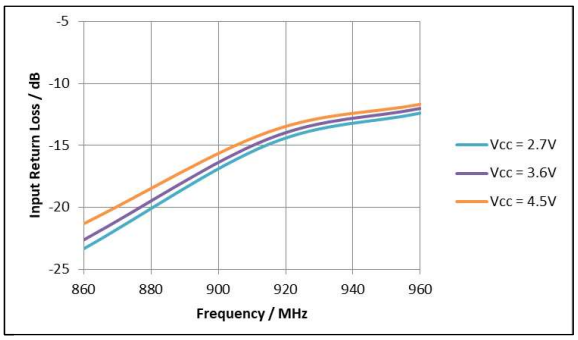


Figure 44 - Input Return Loss (-20 dBm Pin)

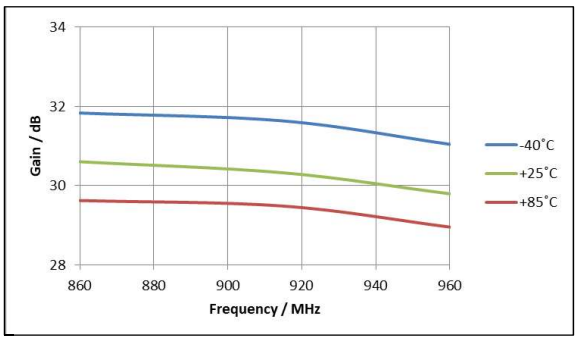


Figure 45 - Gain (-20 dBm Pin)

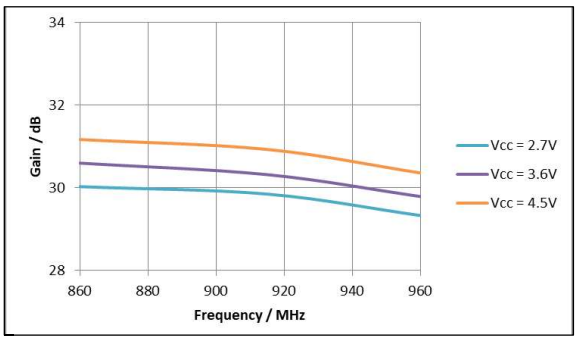


Figure 46 - Gain (-20 dBm Pin)

Test conditions unless otherwise noted:-

Vcc = 3.6 V, Vbias = Vctrl = 3.3 V, Ta = 25 °C, Zo = 50 Ω

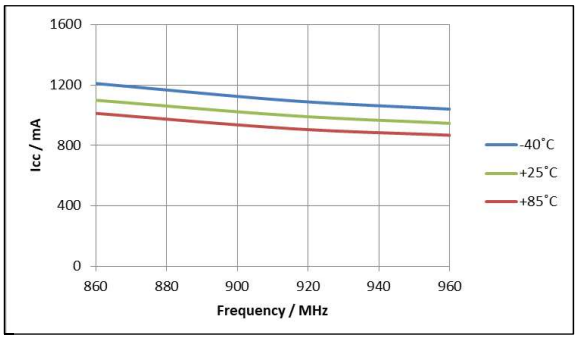


Figure 47 - Icc (+5 dBm Pin)

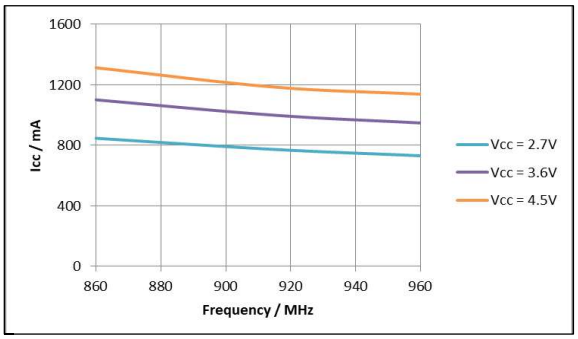


Figure 48 - Icc (+5 dBm Pin)

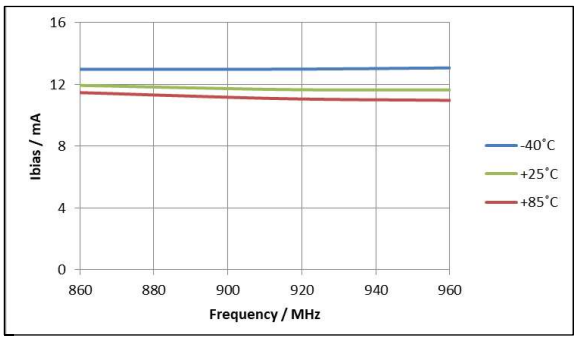


Figure 49 - Ibias (+5 dBm Pin)

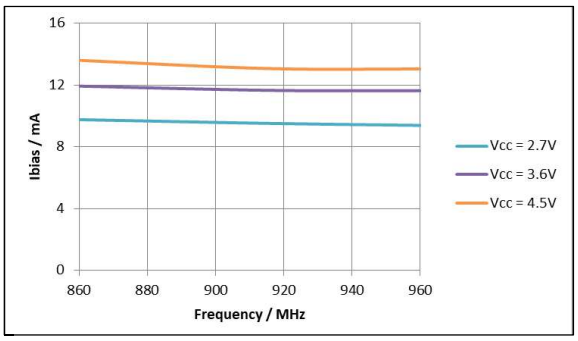


Figure 50 - Ibias (+5 dBm Pin)

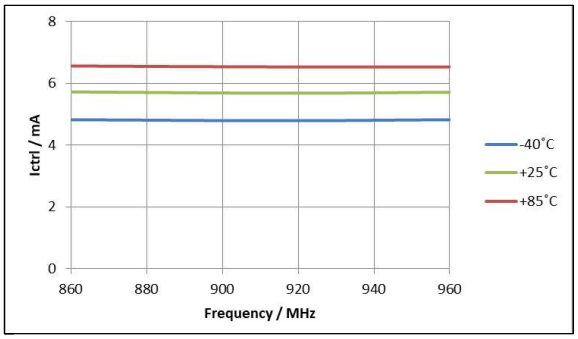


Figure 51 - Ictrl (+5 dBm Pin)

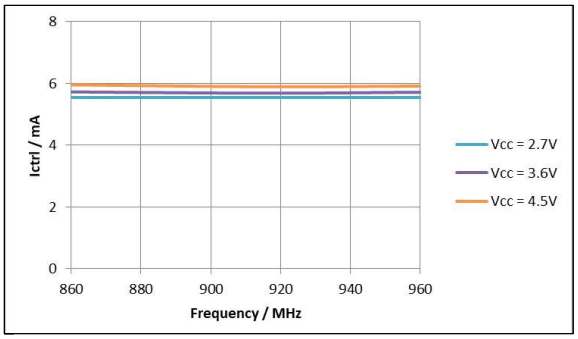


Figure 52 - Ictrl (+5 dBm Pin)

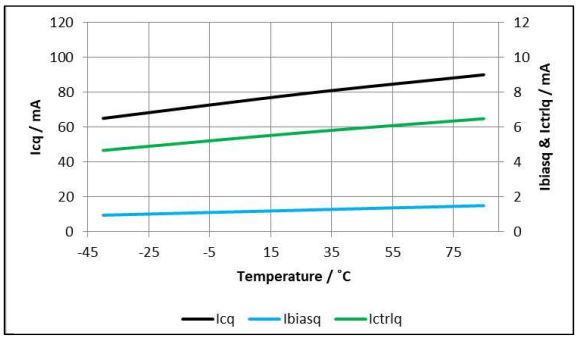


Figure 53 - Quiescent Currents

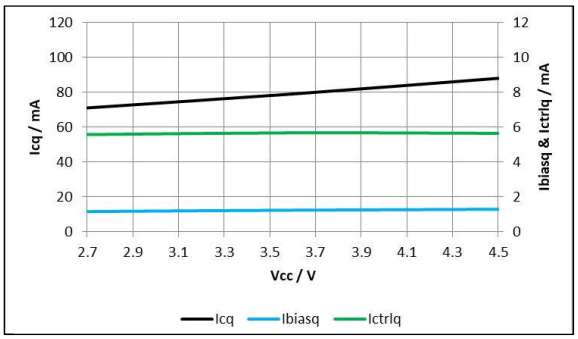


Figure 54 - Quiescent Currents

Test conditions unless otherwise noted:-

Vcc = 3.6 V, Vbias = Vctrl = 3.3 V, Ta = 25 °C, Zo = 50 Ω, Pin = -20 dBm

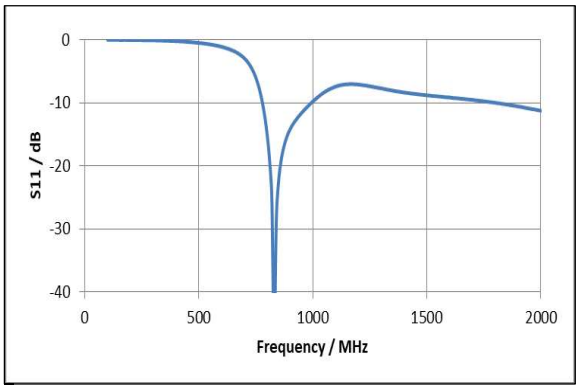


Figure 55 - Input Return Loss (S11)

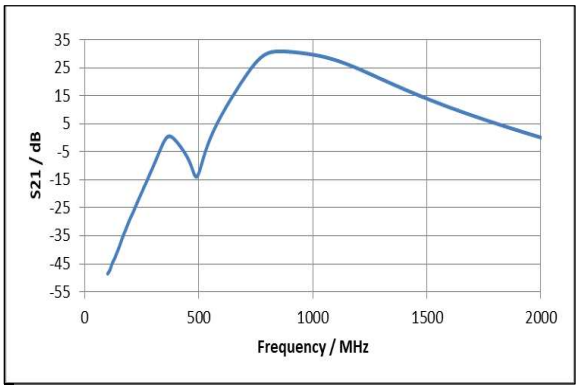


Figure 56 - Small Signal Gain (S21)

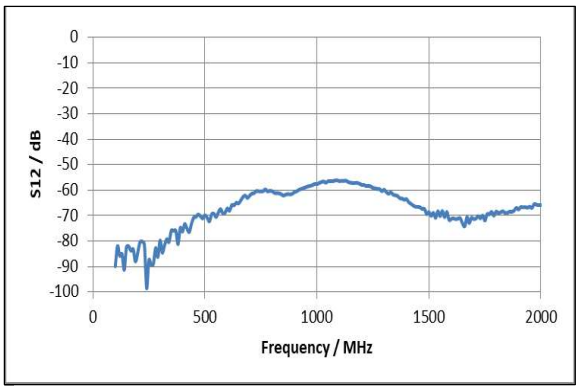


Figure 57 - Reverse Isolation (S12)

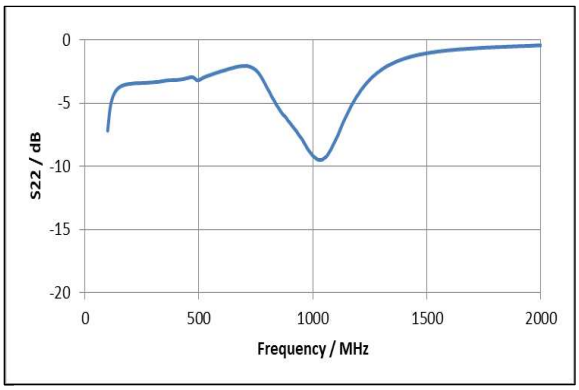


Figure 58 - Output Return Loss (S22)

Application Information

Schematic Diagram

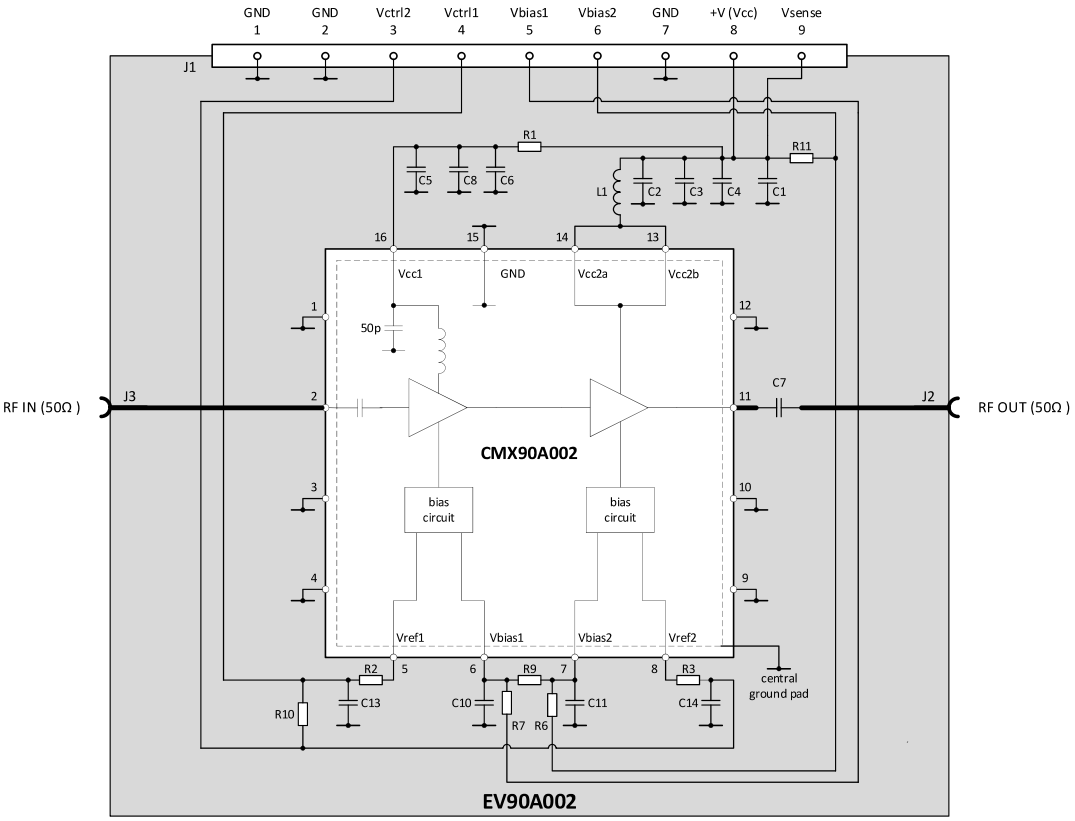


Figure 59 - EV90A002 Schematic

Bill Of Materials (BOM)

Reference Designator	Value	Size	Description
C1	10 uF	0603	X5R, 10 V, ±20 %
C2	47 pF	0402	COG, 25 V, ±5 %
C3	10 nF	0402	X7R, 16 V, ±10 %
C4	DNF		
C5	DNF		
C6	DNF		
C7	100 pF	0402	COG, 25 V, ±5 %
C8	10 nF	0402	X7R, 16 V, ±10 %
C10	1 uF	0402	X5R, 10 V, ±10 %
C11	DNF		
C13	10 nF	0402	X7R, 16 V, ±10 %
C14	10 nF	0402	X7R, 16 V, ±10 %
L1	33 nH	0603	0603AF, ±5 %
R1	0 R	0402	0.063 W, ±1 %
R2	270 R	0402	0.063 W, ±1 %
R3	270 R	0402	0.063 W, ±1 %
R6	DNF		
R7	0 R	0402	0.063 W, ±1 %
R9	0 R	0402	0.063 W, ±1 %
R10	DNF		
R11	DNF		

Notes

- DNF = Do not fit component
- The recommended manufacturer for the inductor (L1) is Coilcraft, manufacturer part # 0603AF-33NXJE.

PCB Layout

Careful layout of the printed circuit board (PCB) is essential for optimum RF and thermal performance. The recommended layout, including ground via pattern underneath the device, may be taken from the evaluation board (Part Number EV90A002). See following section for recommendations on best thermal design.

The PCB consists of four-layer FR-4 with a total thickness of 1.62 mm (Figure 60) and the EV90A002 PCB (Figure 61) is 50 mm x 50 mm. The microstrip RF input and output width is 0.35 mm.

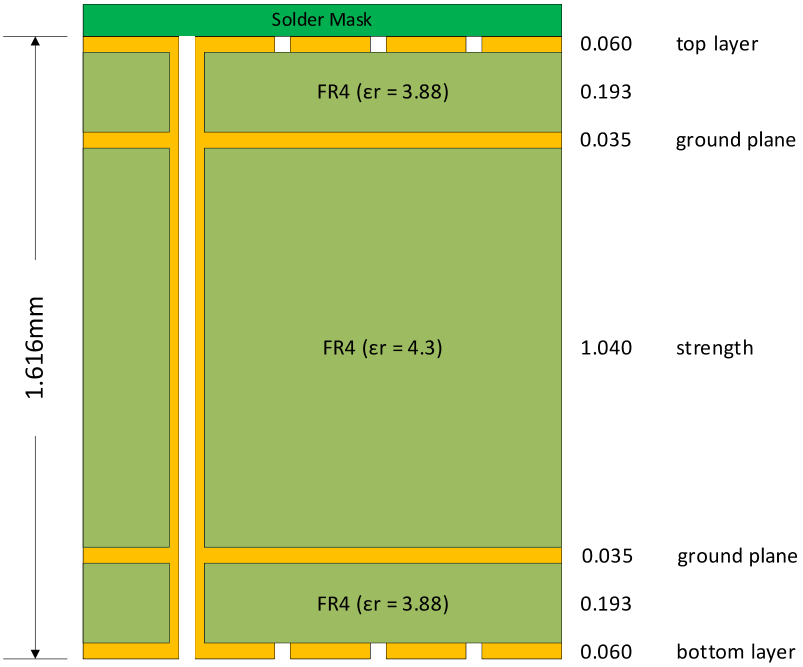


Figure 60 - EV90A002 PCB Layer Stack

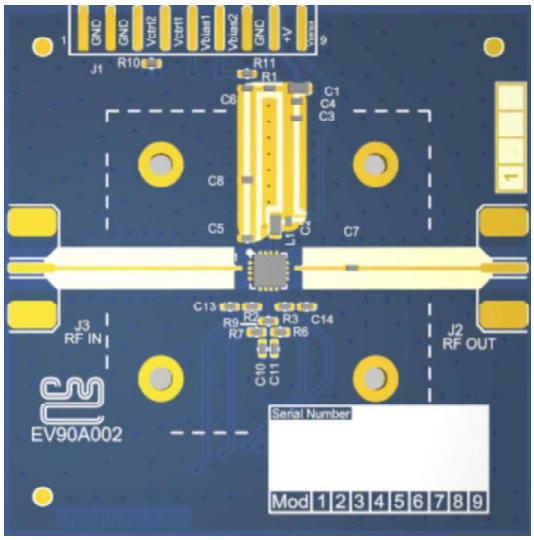


Figure 61 - EV90A002 PCB Top Layer View

Thermal Design

The primary RF/DC ground and thermal path is via the exposed die pad on the backside of the package, which must be connected to the PCB ground plane. An array of plated through-hole vias directly underneath the die pad area is essential to conduct heat away and minimise ground inductance. A typical solution should have 9 grounding vias connecting the top layer to the bottom layer, with inner diameter of 0.2 mm (and 0.025 mm plating) on 0.875 mm grid pattern. The vias do not need to be filled. The PCB layout should provide a thermal radiator appropriate for the intended operation, adding as much copper to inner and outer layers as possible to avoid excessive junction temperature.

Device junction temperature (Tj) can be calculated using Tj = Tc + (Pdiss x Rjc), where Pdiss = Pdc + Pin - Pout and Tc is the case temperature on the backside of the package (die pad) in contact with the PCB.

A heatsink should be used if the thermal performance of the PCB layout is not adequate and particularly if the user is running the device continuous at Psat. The heatsink should be attached to the rear of the PCB using mounting screws positioned close to the device to ensure good contact with the ground via pattern. The backside of the PCB is clear of solder resist to enable a heatsink to be applied.

A low inductance connection as described between the central ground pad and the board RF ground plane prevents unwanted gain peaking and instability due to internal ground path feedback.

Vref Pins

The quiescent bias current of each stage is proportional to the current into the associated Vref pin. This current is set by a series resistor from the Vctrl regulated supply. These resistors are 270 Ω on the EV90A002, resulting in the following currents:

- Current into Vref1 = (Vctrl1 – 2.40) / (270 + 54.0) = 2.78 mA (with Vctrl1 = 3.3 V)
- Current into Vref2 = (Vctrl2 – 2.40) / (270 + 42.5) = 2.88 mA (with Vctrl2 = 3.3 V)

These bias points have been selected for optimum PA efficiency. It is possible to achieve these same currents from higher or lower Vctrl supplies by appropriate selection of the series resistors. To ensure correct bias circuit operation the current into either Vref1 or Vref2 should not exceed 5mA.

The device can be placed into standby mode when not in use by setting Vctrl low (<1.5 V) to disable the bias circuits. Vctrl can also be used to ramp the CMX90A002 output power up or down to support burst signals and TDD systems. By varying Vref between 1.5 V and 2.5 V (typ.) the output power can be adjusted by more than >65 dB (Figure 62). Controlling each Vctrl input separately contributes approximately half of the total control range.

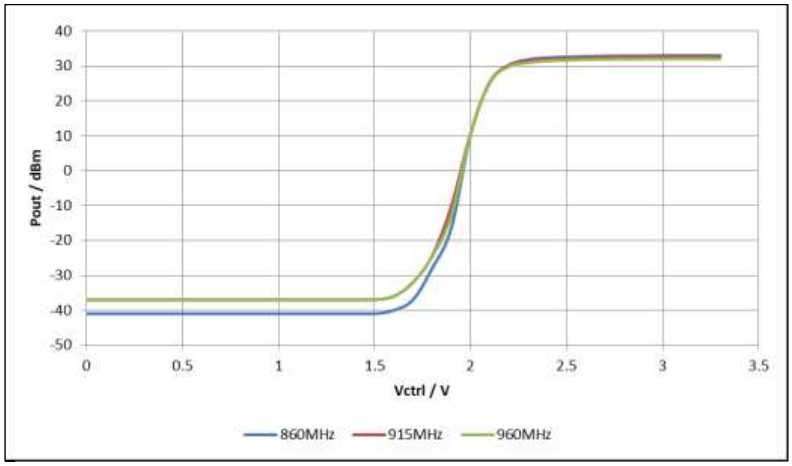


Figure 62 - Vctrl Power Control

Vbias Pins

The Vbias pins provide the supply to the bias circuits and the associated base current to the two amplifier stages. To consolidate power supplies the Vbias pins can be connected to Vcc without affecting the performance of the device. The output power performance with Vbias connected to Vcc is compared with Vbias connected to a fixed 3.3 V supply.

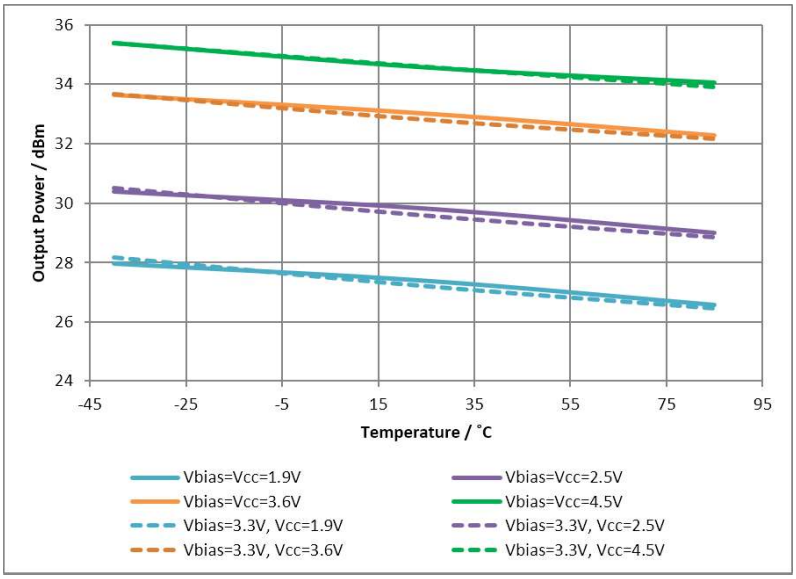


Figure 63 - Output Power (Vbias = Vcc)

Evaluation Board and Bias Procedure

Ensure an adequately rated attenuator is placed between the output of the amplifier (RFout) and 50 Ω RF test equipment. The amplifier RFin should be connected to a signal generator with RF off. A dual power supply will be needed, with output of +3.6 V @ 2 A for the collector voltage (Vcc) and +3.3 V @ 100 mA for the bias circuitry (Vbias and Vref). Use good quality cables to minimise any voltage drop between the PSU and evaluation board. Connect the power supply with RF off and ensure that the evaluation board consumes the correct quiescent current (Icq). Although it is good practice to enable the Vcc supply before the bias circuitry, in general, power supply sequencing is not necessary. If the quiescent current is correct, enable the RF signal with a low level RFin = -30 dBm to begin with to ensure the device is not overdriven. Ensure the test signal is within the recommended frequency range of the device and that the output signal measured on the test equipment complies with small signal gain, before continuing with any further tests.

Standard power supply connections

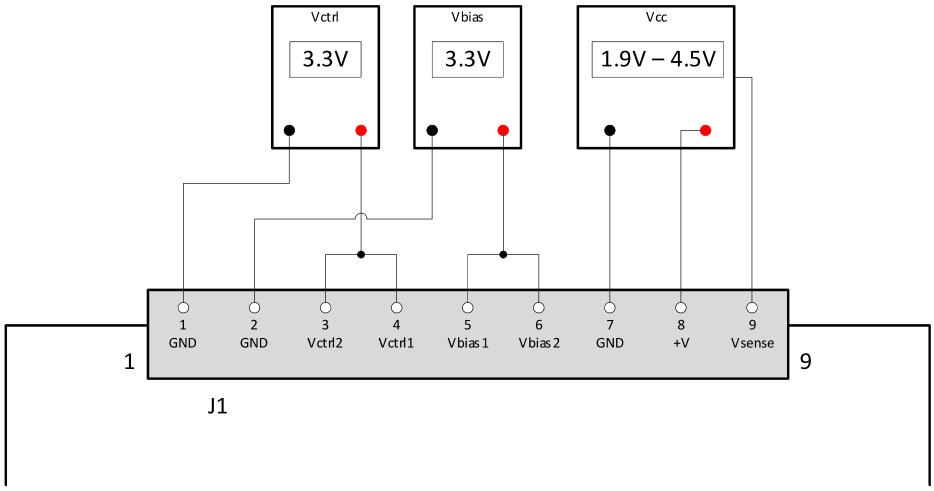


Figure 64 - Standard Power Supply Connections

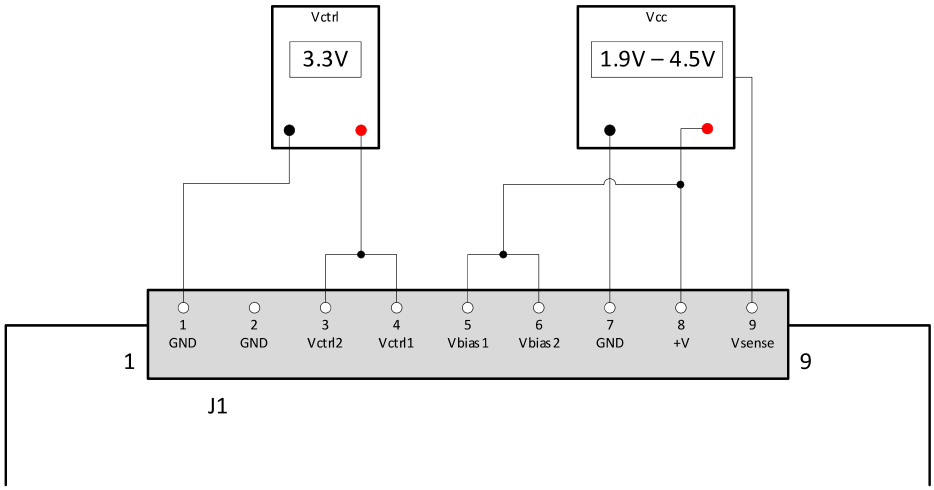


Figure 65 - Alternative Power Supply Connections with Vbias = Vcc

Ruggedness

To prevent possible damage to the device, care should be taken to ensure that the VSWR of the load that the CMX90A002 is working into does not exceed the limits in the Electrical Specification.

The maximum possible supply voltage should be taken into account when designing with the CMX90A002 PA. This is particularly important when Vcc is derived from a battery that can have a higher voltage than nominal when fully charged, for example a 3.6 V Li-ion battery at full charge is usually at 4.2 V.

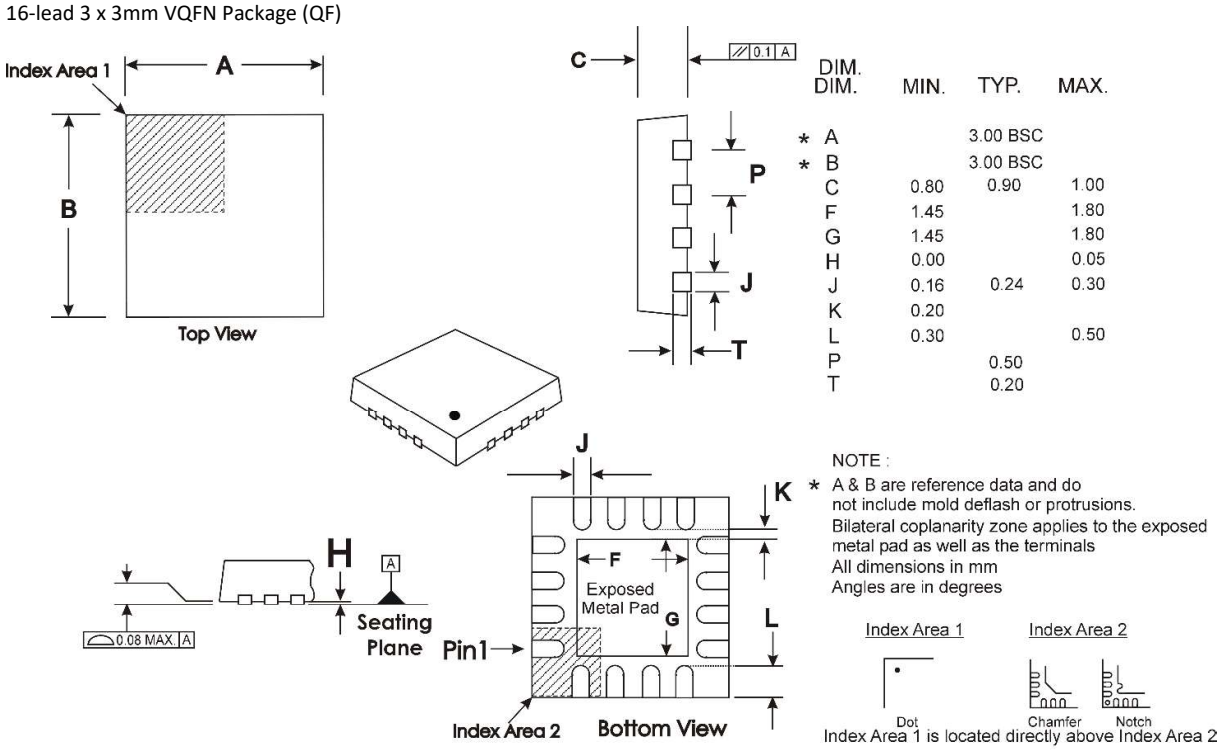
A typical transmit system will have filtering, transmit/receive switching and antenna matching between the PA and the antenna. These all need to be designed carefully to ensure a good 50 Ω match is presented to the PA that is above the minimum return loss limits over the whole operating frequency range.

External effects on the antenna impedance should also be taken into account. Proximity to other objects and surfaces can change the antenna impedance significantly, resulting in the return loss presented to the PA falling below the limit and therefore subsequent damage to the PA.

If there is an external antenna connector on the equipment, it should be assumed that the wrong antenna might get connected or that the transmitter may be operated with no antenna connected. To avoid the resulting high VSWR damaging the PA additional protection such as a circulator may be necessary.

Package Outline

16-lead 3 x 3mm VQFN Package (QF)



DIM. DIM.	MIN.	TYP.	MAX.
* A		3.00 BSC	
* B		3.00 BSC	
C	0.80	0.90	1.00
F	1.45		1.80
G	1.45		1.80
H	0.00		0.05
J	0.16	0.24	0.30
K	0.20		
L	0.30		0.50
P		0.50	
T		0.20	

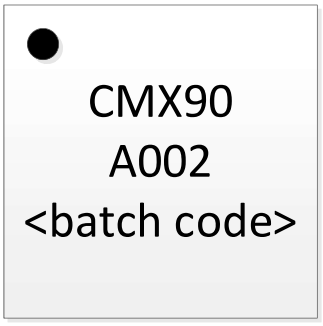
NOTE :
* A & B are reference data and do not include mold deflash or protrusions.
Bilateral coplanarity zone applies to the exposed metal pad as well as the terminals
All dimensions in mm
Angles are in degrees

Index Area 1 is located directly above Index Area 2

The underside of the package has an exposed metal pad which should be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Package Marking

Pin 1 indicator (dot) and 3 rows of text for device identification.



Line 1: CMX90 SµRF series

Line 2: 4-character part code

Line 3: Batch code

Revision History

Issue	Description	Date
1	First public release	September 2026

ROHS Compliance

CML Micro certifies, to the best of our knowledge, that its products comply with **RoHS directive (2011/65/EU)**, as amended by **Directive (EU) 2015/863.**

REACH Compliance

CML Micro certifies, to the best of our knowledge, that its products do not contain any of the banned substances specified in the SVHC list at https://echa.europa.eu/candidate-list-table. CML Micro are committed to ensuring the safety of products and the compliance with regulations. Publications will be updated in the event that REACH control is compromised.

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Contact details can be found at www.cmlmicro.com

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