Provisional Issue

CMX90A007 2W 136 – 1000 MHz 2-stage Driver Amplifier

Description

The CMX90A007 is a high gain two-stage GaAs HBT driver amplifier in a plastic QFN package, delivering +33.5 dBm (2.2 W) of output power with >50 % efficiency at 435 MHz and 7.4 V.

CMX90A007 requires external matching at both input and output to optimize performance for each application and frequency band. The measured data presented in this document is based on the evaluation board (EV90A007).

The wide supply voltage range of 6 – 9.5 V makes the CMX90A007 suitable for a variety of applications and enables direct connection to dual-cell Lithium batteries. The integrated active bias circuit and wideband interstage match ease design effort and minimize external components and PCB area.

CMX90A007 can be used as a stand-alone final stage PA or driver stage for the CMX90A009.

Applications

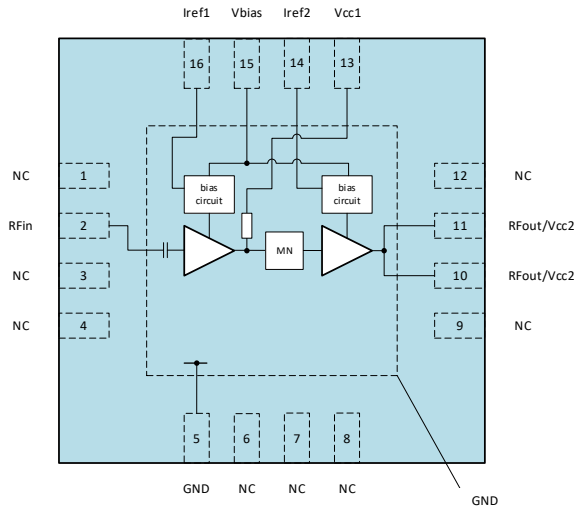
- Critical communications
- PMR / LMR hand-portable
- Two-way radio (analogue / digital)
- Public safety TETRA / P25
- Wireless data modem / network
- VHF / UHF / 915 MHz ISM band
- Marine radio / AIS

4x4mm VQFN-16 Package

Product Features

- Frequency range 136 – 1000 MHz
- Supply voltage 6 – 9.5 V
- P3dB +33.5 dBm @ 435 MHz, Vcc = 7.4 V
- Small signal gain 27 dB
- High collector efficiency 53 % @ P3dB
- On-chip active bias and interstage match
- Saturated and linear operation
- OIP3 +45 dBm @ +27 dBm/tone @ 435 MHz

Block Diagram



Ordering Information

Part Number	Description
CMX90A007Q7-R710	7” Reel with 1,000 pieces
CMX90A007Q7-R350	13” Reel with 5,000 pieces
EV90A007	Evaluation board (400-470MHz)

Absolute Maximum Ratings

Parameter	Rating
RF Input Power	+13 dBm
Device Voltage (Vcc1, Vcc2)	+10 V
Case Temperature (Tc)	-40 to +85 °C
Junction Temperature (Tjmax)	200 °C (MTTF = 10^6 hours)
Storage Temperature	-40 to +125 °C
ESD Sensitivity	HBM >250 V (Class 1A); CDM >1 kV (Class C3)
MSL Level	Level 3

Exceeding the maximum ratings may result in damage or reduced device reliability.

Thermal Characteristics

Parameter	Rating
Thermal Resistance (Rjc)	33.8 °C/W at Tc = 85 °C

Thermal resistance is junction-to-case, where case refers to the exposed die pad on the backside which is in contact with the board.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Operating Frequency Range	136		1000	MHz
Case Temperature (Tc)	-40		+85	°C
Device Voltage (Vcc1, Vcc2)	6.0	7.4	9.5	V
Bias Voltage (Vbias)	6.0	7.4	9.5	V

The device will be tested under certain conditions, but performance is not guaranteed over the full range of recommended operating conditions.

ESD Caution

CMX90A007 incorporates ESD protection circuitry. However, ESD precautions are strongly recommended for handling and assembly. Ensure that devices are protected from ESD in antistatic bags or carriers when being transported. Personal grounding is to be worn at all times when handling these devices.

RoHS Compliance

All devices and evaluation kits supplied by CML Micro are compliant with RoHS directive (2011/65/EU), containing less than the permitted levels of hazardous substances.

Electrical Specification

Measured results on the EV90A007 evaluation board including PCB losses. Matching optimised for specified operating band or frequency.

Vcc = Vbias = +7.4 V, Vref = +3.15V (Vref = Vref1 = Vref2), Icq = Icc + Ibias, Ta = +25 °C (unless otherwise noted)

Parameter	Conditions	Notes	Min	Typ	Max	Units
Standby Current	Vcc current in standby mode, RF OFF			< 5		uA
Vbias Current	RF OFF			0.7		mA
Vref1, 2 (Standby)	PA placed into standby mode		0		1.5	V
Vref Current	Vref1 & 2 total current. See applications section for further details.	1		1.5		mA

Notes
1. Bias setting resistors as application circuit in application information section, R14 and R16 in Figure 50.

Operating Characteristics 400 - 470 MHz

Zo = 50 Ω, Vcc = Vbias = +7.4 V, Vref = +3.15V (Vref = Vref1 = Vref2), Ta = +25 °C (unless otherwise noted)

Parameter	Conditions	Notes	Min	Typ	Max	Units
Frequency			400		470	MHz
P3dB				33.5		dBm
Psat				34.2		dBm
Small Signal Gain	Pin = -20 dBm			27		dB
Large Signal Gain	435 MHz, P3dB			24		dB
Collector Efficiency (η)	435 MHz, P3dB			53		%
OIP3	435 MHz, Pout = +27 dBm/tone			45		dBm
Quiescent Current (Icq)	RF OFF	1		49.5		mA
Current Consumption (Icc)	435 MHz, P3dB			0.56		A
Vbias Current (Ibias)	435 MHz, P3dB			9		mA
Noise Figure	435 MHz			10.2		dB
Input Return Loss	Pin = -20 dBm			20		dB
2nd Harmonic (2Fo)	435 MHz, P3dB			-40		dBc
3rd Harmonic (3Fo)	400 MHz, P3dB			-50		dBc
Load Ruggedness	P3dB, all phase angles, Vcc = Vbias = 7.4 V			>10:1		VSWR
Turn-On Time	Vref = 0 V to 4 V			TBD		ns
Turn-Off Time	Vref = 4 V to 0 V			TBD		ns

Operating Characteristics 136 - 174 MHz

Zo = 50 Ω, Vcc = Vbias = +7.4 V, Vref = +3.15V (Vref = Vref1 = Vref2), Ta = +25 °C (unless otherwise noted)

Parameter	Conditions	Notes	Min	Typ	Max	Units
Frequency			136		174	MHz
P3dB				35		dBm
Psat				35.3		dBm
Small Signal Gain	Pin = -20 dBm			32		dB
Large Signal Gain	155 MHz, P3dB			29		dB
Collector Efficiency (η)	155 MHz, P3dB			58		%
OIP3	155 MHz, Pout = +27 dBm/tone			43		dBm
Quiescent Current (Icq)	RF OFF	2	-	43	-	mA
Current Consumption (Icc)	155 MHz, P3dB			0.7		A
Vref Current	Vref1 & 2 total current	2		1.1		mA
Vbias Current (Ibias)	155 MHz, P3dB			12		mA
Input Return Loss	155 MHz, Pin = -20 dBm			25		dB
2nd Harmonic (2Fo)	155 MHz, P3dB			-30		dBc
3rd Harmonic (3Fo)	155 MHz, P3dB			-45		dBc

Notes
2. Bias setting resistors, R14 and R16 in Figure 50, are both 953Ω, see applications section for further details.

Operating Characteristics 900 - 930 MHz

Zo = 50 Ω, Vcc = Vbias = +7.4 V, Vref = +3.15V (Vref = Vref1 = Vref2), Ta = +25 °C (unless otherwise noted)

Parameter	Conditions	Notes	Min	Typ	Max	Units
Frequency			900		930	MHz
P3dB				33.5		dBm
Psat				34.8		dBm
Small Signal Gain	Pin = -20 dBm			25		dB
Large Signal Gain	915 MHz, P3dB			22		dB
Collector Efficiency (η)	915 MHz, P3dB			50		%
OIP3	915 MHz, Pout = +27 dBm/tone			45		dBm
Quiescent Current (Icq)	RF OFF	3	-	77	-	mA
Current Consumption (Icc)	915 MHz, P3dB			0.68		A
Vref Current	Vref1 & 2 total current	3		2.8		mA
Vbias Current (Ibias)	915 MHz, P3dB			10		mA
Input Return Loss	Pin = -20 dBm			25		dB
2nd Harmonic (2Fo)	915 MHz, P3dB			-30		dBc
3rd Harmonic (3Fo)	915 MHz, P3dB			-50		dBc

Notes
3. Bias setting resistors, R14 and R16 in Figure 50, are both 316Ω, see applications section for further details.

Pin Assignments

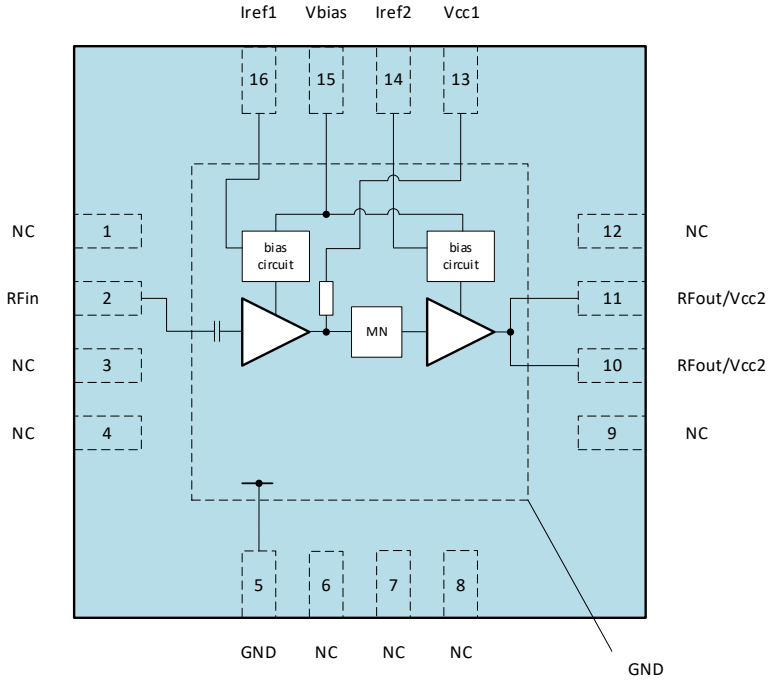


Figure 1 - Top View

Pin	Name	Description
1	NC	Connect to GND
2	RFin	RF input. An external input match to 50 Ω is required. Internally DC blocked.
3	NC	Connect to GND
4	NC	Connect to GND
5	NC	Connect to GND
6	NC	Connect to GND
7	NC	Connect to GND
8	NC	Connect to GND
9	NC	Connect to GND
10	RFout/Vcc2	RF output. External matching to 50 Ω and DC-blocking capacitor required. Vcc2 (final stage) to be applied using external bias feed. Pin 10 & 11 to be connected on PCB.
11	RFout/Vcc2	RF output. External matching to 50 Ω and DC-blocking capacitor required. Vcc2 (final stage) to be applied using external bias feed. Pin 10 & 11 to be connected on PCB.
12	NC	Connect to GND
13	Vcc1	Collector supply to first stage. Suitable RF choke required.
14	Iref2	Sets bias current to second stage. Regulated voltage and external series resistor required. Can also be used for on/off and power control.
15	Vbias	Supplies current to both bias circuits.
16	Iref1	Sets bias current to first stage. Regulated voltage and external series resistor required. Can also be used for on/off and power control.
Die pad	GND	DC and RF ground. Exposed die pad must be connected to GND.

Notes

CML recommends that all no connect (NC) pins are connected to ground.

The bottom exposed die pad must be connected to the ground plane on the board, note guidance given in the application information section.

Typical Performance

The following plots show typical performance characteristics of CMX90A007 measured on the evaluation board (Part Number - EV90A007).

Test conditions unless otherwise noted:-

Vcc = Vbias = +7.4 V, Vref = Vref1 = Vref2 = +3.15 V, Ta = +25 °C, Zo = 50 Ω.

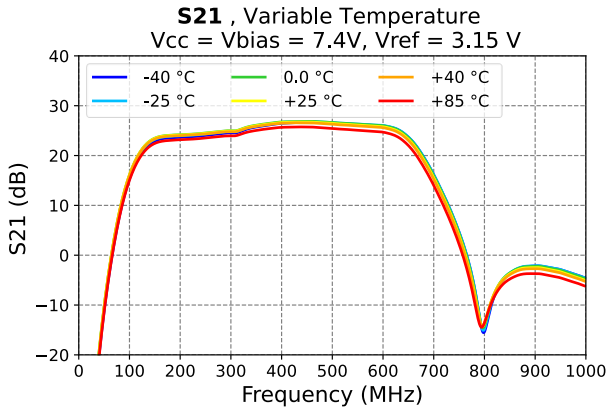


Figure 2 - Small Signal Gain (S21)

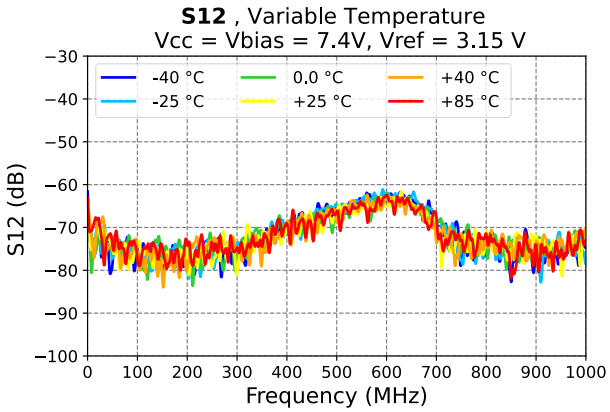


Figure 3 - Reverse Isolation (S12)

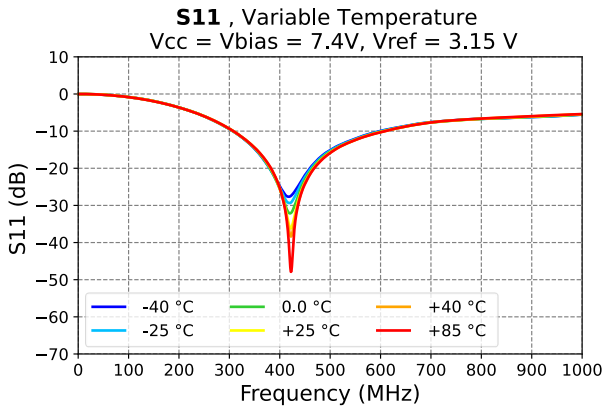


Figure 4 - Input Return Loss (S11)

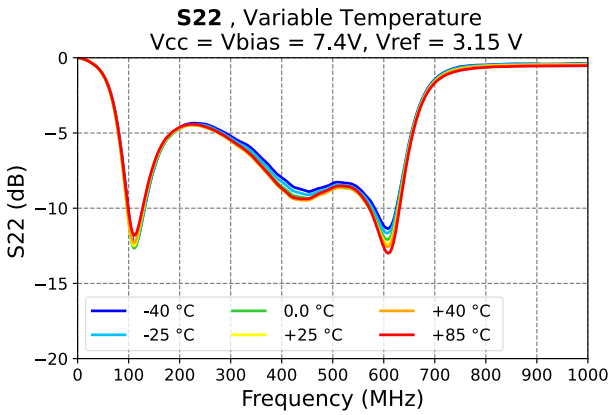


Figure 5 - Output Return Loss (S22)

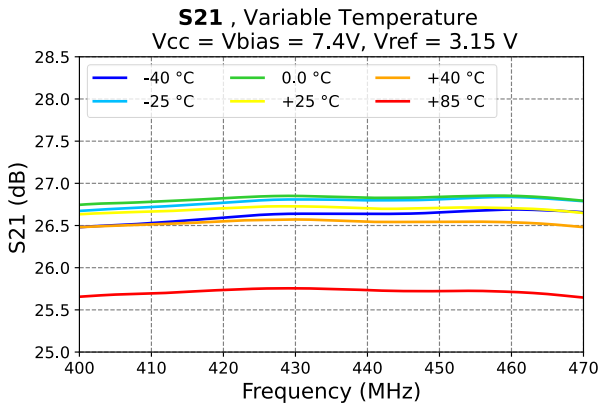


Figure 6 - Small Signal Gain (S21)

Test conditions unless otherwise noted:-

Vcc = Vbias = +7.4 V, Vref = Vref1 = Vref2 = +3.15 V, Ta = +25 °C, Zo = 50 Ω.

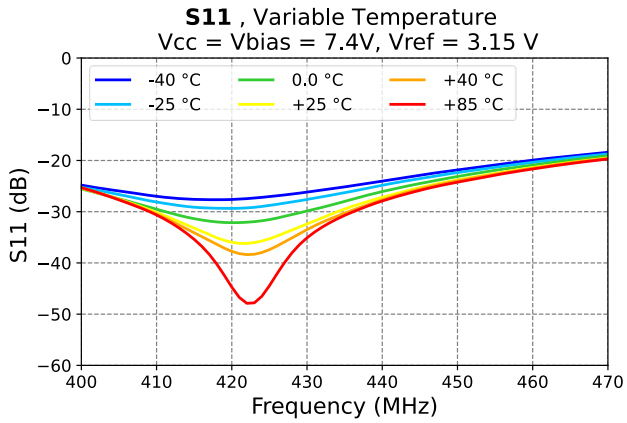


Figure 7 - Input Return Loss (S11)

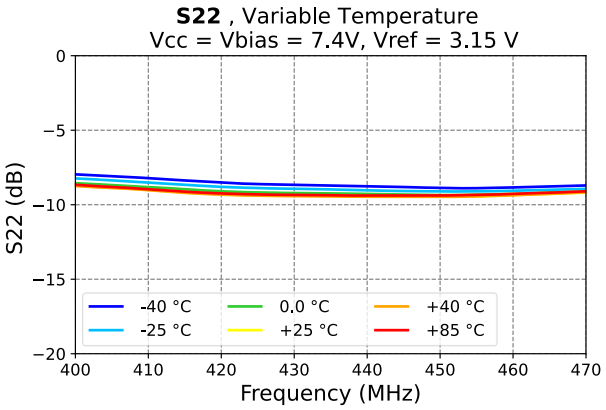


Figure 8 - Output Return Loss (S22)

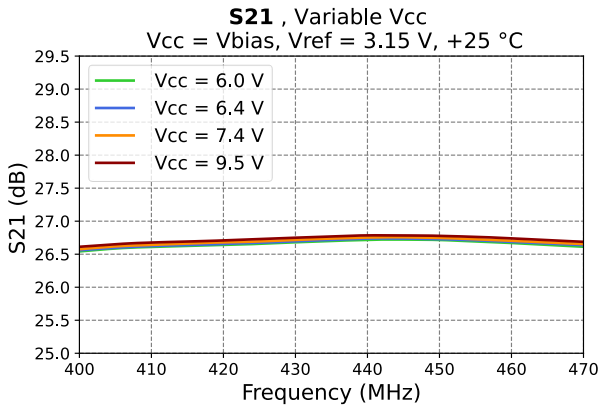


Figure 9 - Small Signal Gain vs. Vcc

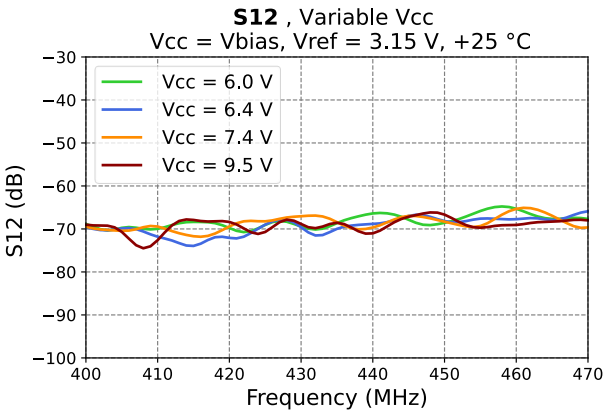


Figure 10 - Reverse Isolation vs. Vcc

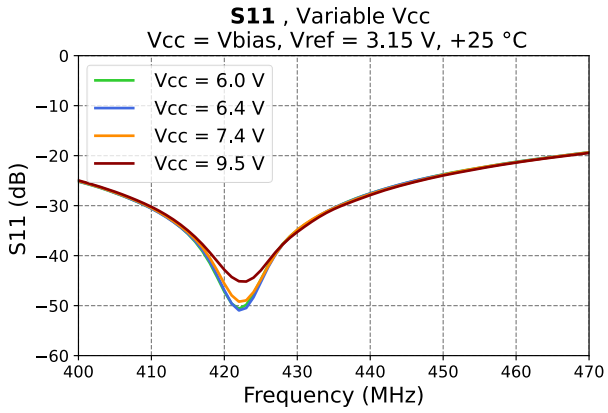


Figure 11 - Input Return Loss vs. Vcc

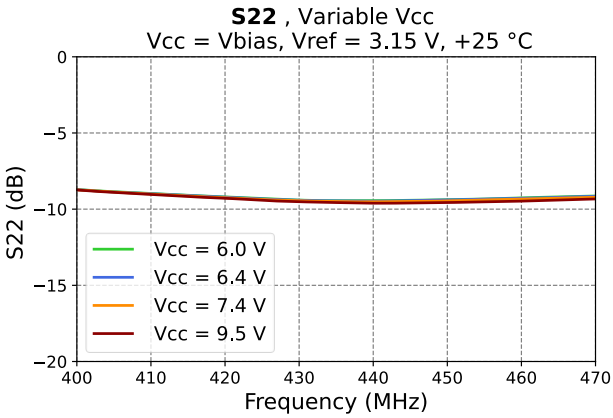


Figure 12 - Output Return Loss vs. Vcc

Test conditions unless otherwise noted:-
Vcc = Vbias = +7.4 V, Vref = Vref1 = Vref2 = +3.15 V, Ta = +25 °C, Zo = 50 Ω.

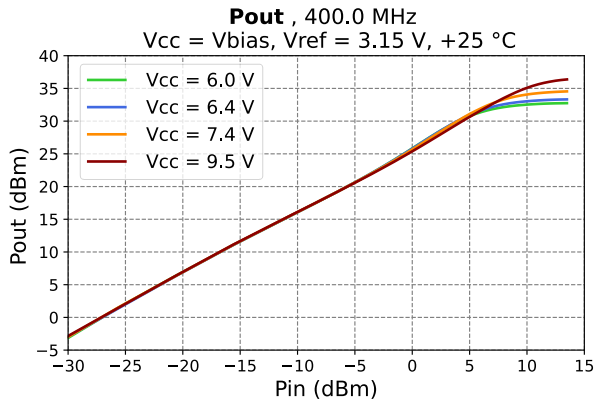


Figure 13 - Output Power vs. Input Power at 400 MHz

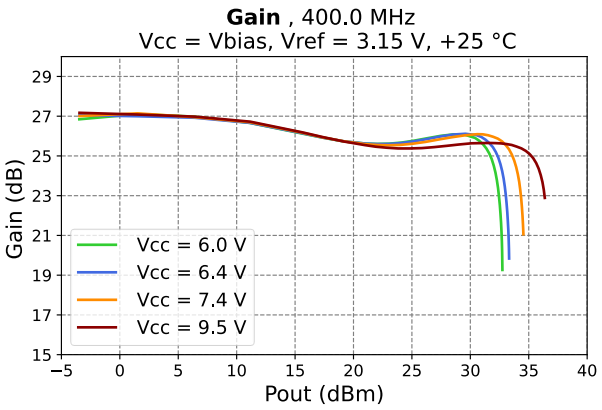


Figure 14 - Gain vs. Output Power at 400 MHz

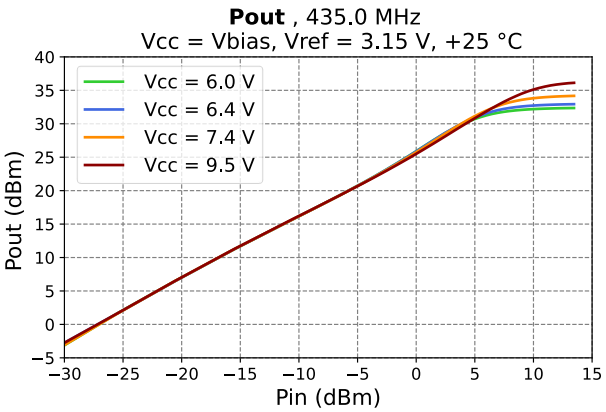


Figure 15 - Output Power vs. Input Power at 435 MHz

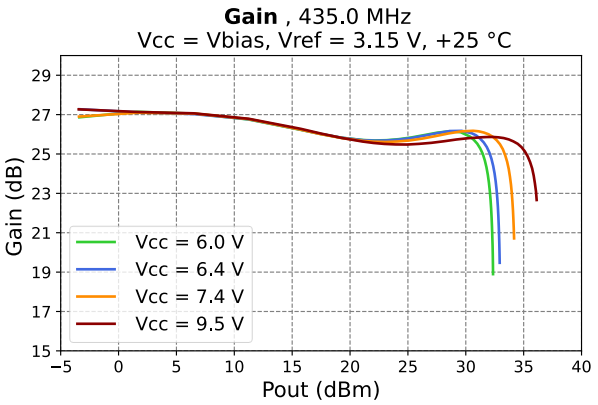


Figure 16 - Gain vs. Output Power at 435 MHz

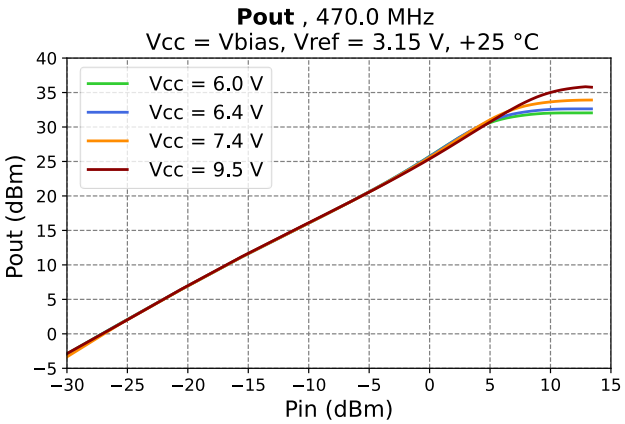


Figure 17 - Output Power vs. Input Power at 470 MHz

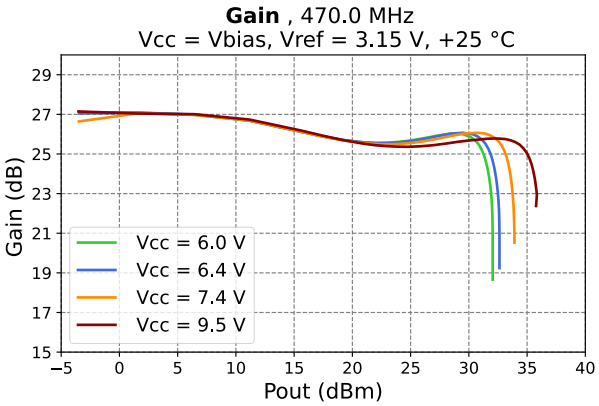


Figure 18 - Gain vs. Output Power at 470 MHz

Test conditions unless otherwise noted:-
Vcc = Vbias = +7.4 V, Vref = Vref1 = Vref2 = +3.15 V, Ta = +25 °C, Zo = 50 Ω.

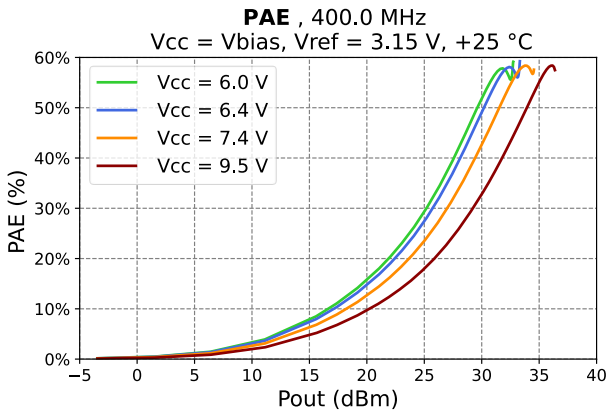


Figure 19 - PAE vs. Output Power at 400 MHz

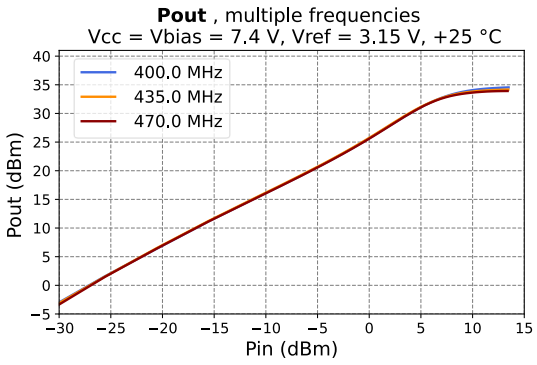


Figure 20 - Output Power vs. Input Power

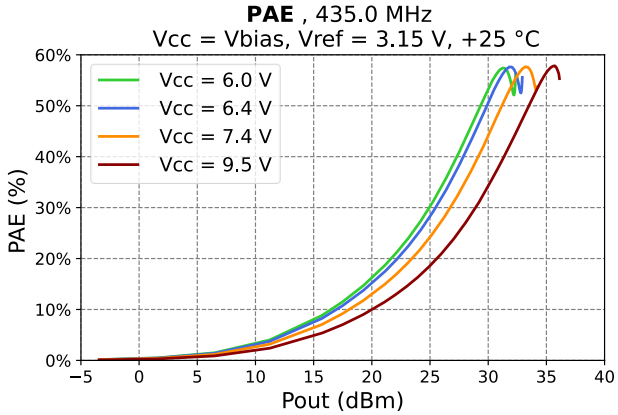


Figure 21 - PAE vs. Output Power at 435 MHz

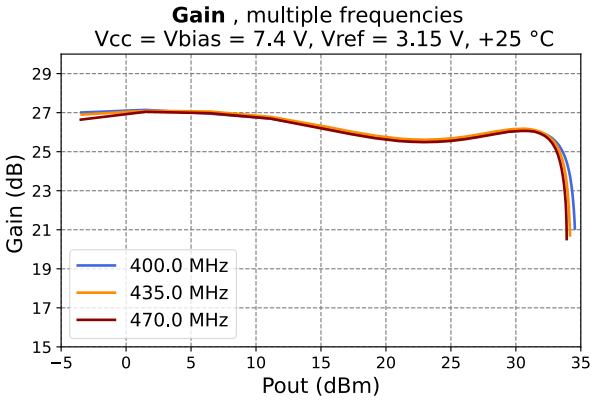


Figure 22 - Gain vs. Output Power

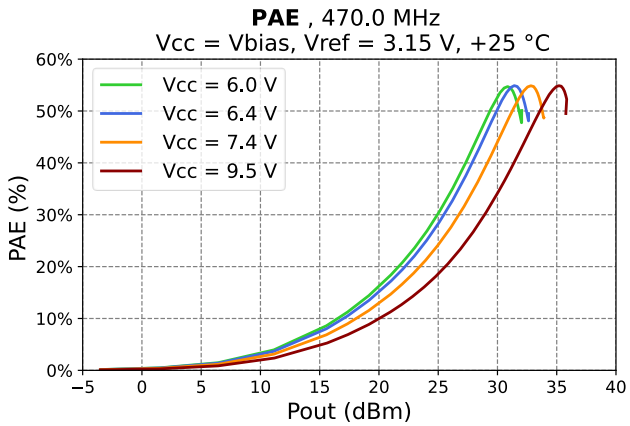


Figure 23 - PAE vs. Output Power at 470 MHz

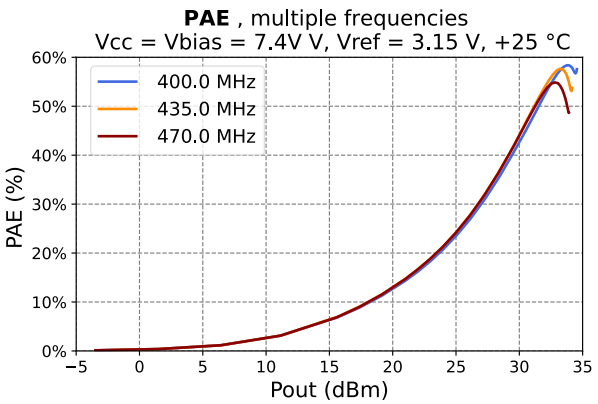


Figure 24 - PAE vs. Output Power

Test conditions unless otherwise noted:-

Vcc = Vbias = +7.4 V, Vref = Vref1 = Vref2 = +3.15 V, Ta = +25 °C, Zo = 50 Ω.

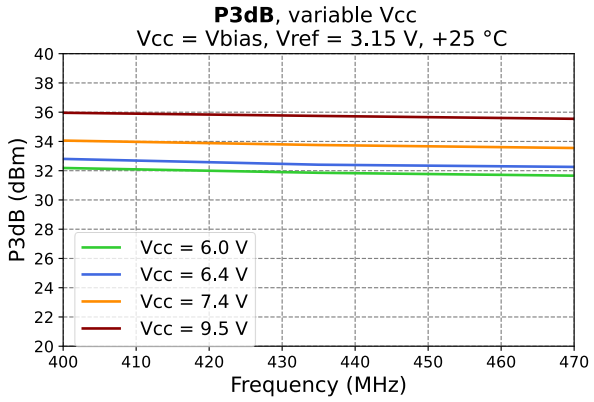


Figure 25 – P3dB vs. Frequency

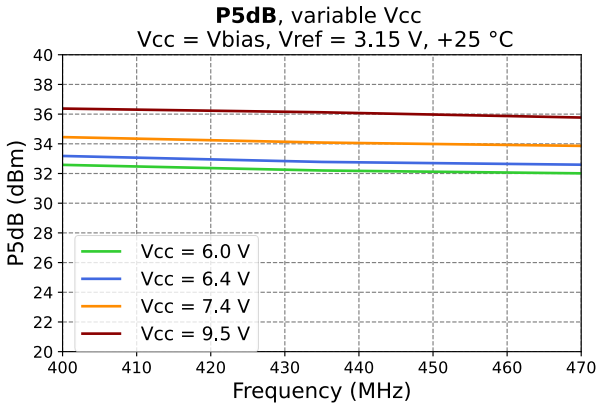


Figure 26 – P5dB vs. Frequency

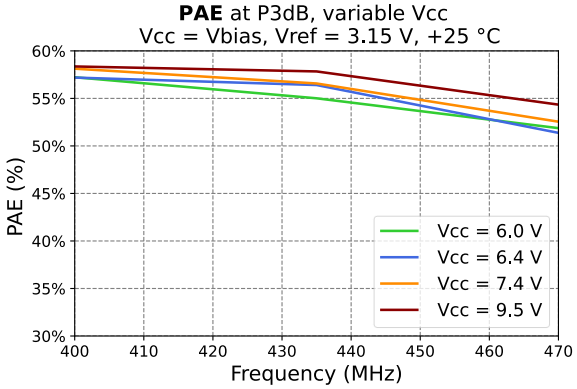


Figure 27 - PAE at P3dB

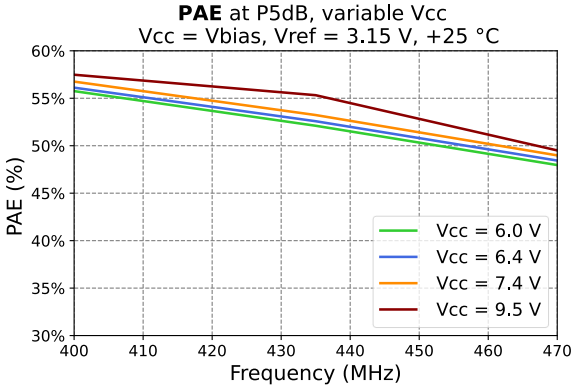


Figure 28 - PAE at Psat

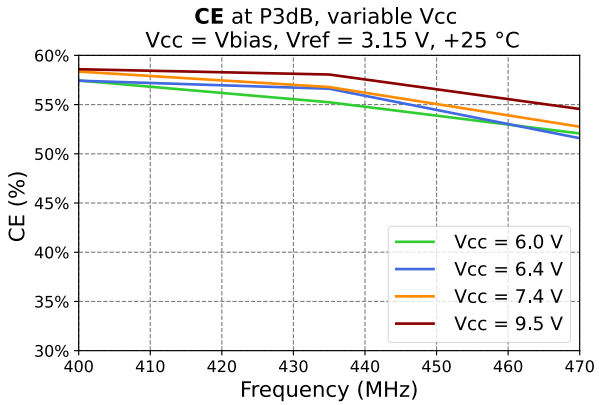


Figure 29 - CE at P3dB

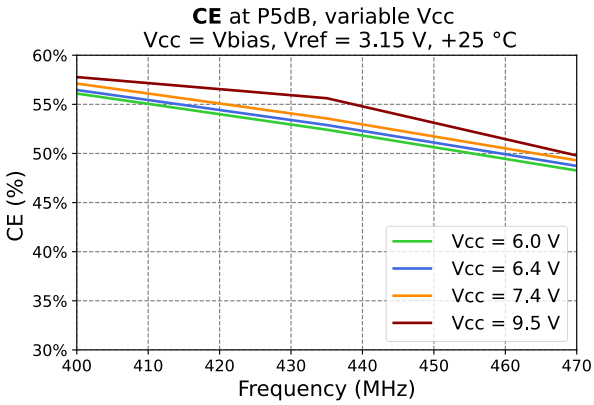


Figure 30 - CE at Psat

Test conditions unless otherwise noted:-
Vcc = Vbias = +7.4 V, Vref = Vref1 = Vref2 = +3.15 V, Ta = +25 °C, Zo = 50 Ω. Iref = Iref1+Iref2

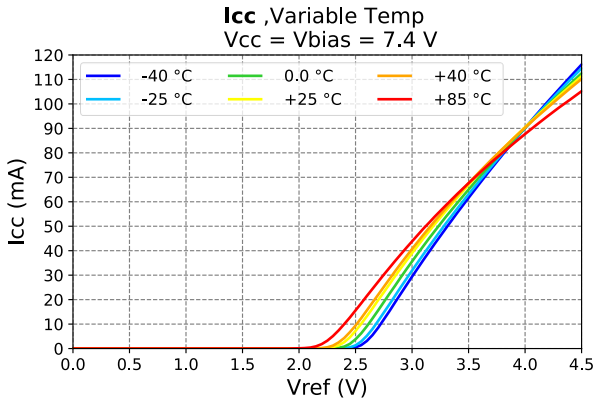


Figure 31 - Icc vs. Vref over Temp

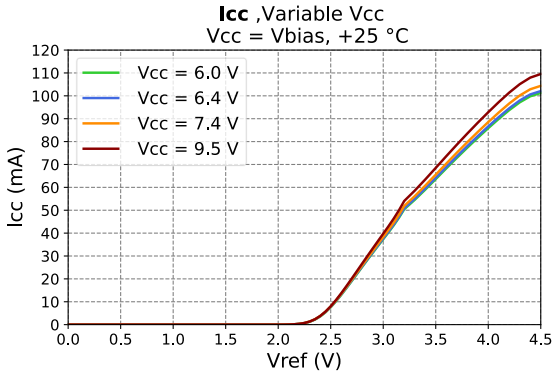


Figure 32 - Icc vs. Vref over Vcc

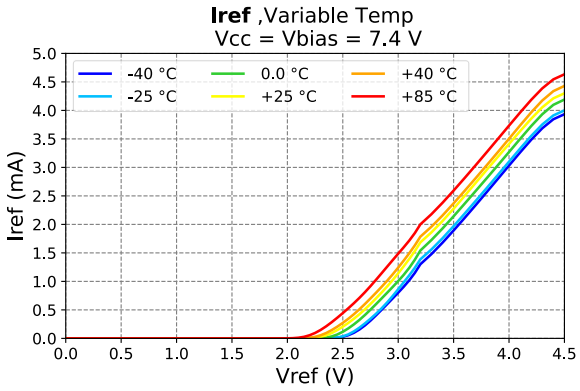


Figure 33 – Iref vs. Vref over Temp

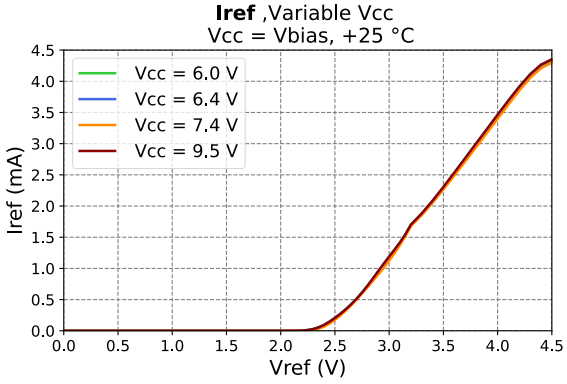


Figure 34 - Iref vs. Vref over Vcc

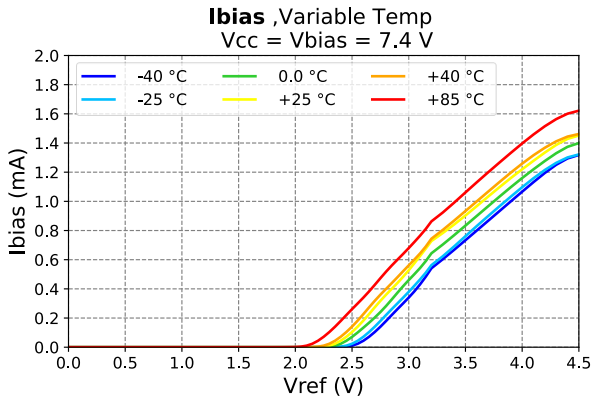


Figure 35 - Ibias vs. Vref over Temp

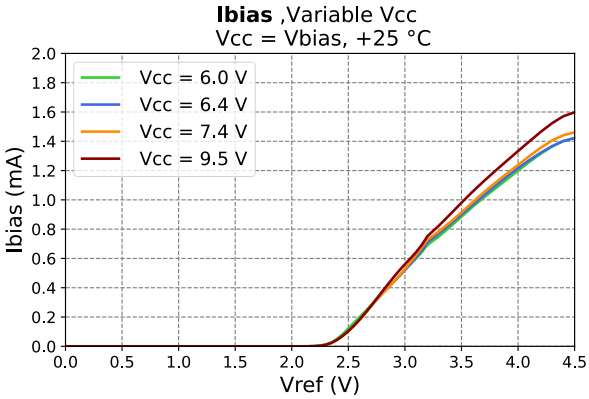


Figure 36 - Ibias vs. Vref over Vcc

Test conditions unless otherwise noted:-

Vcc = Vbias = +7.4 V, Vref = Vref1 = Vref2 = +3.15 V, Ta = +25 °C, Zo = 50 Ω. Iref = Iref1+Iref2

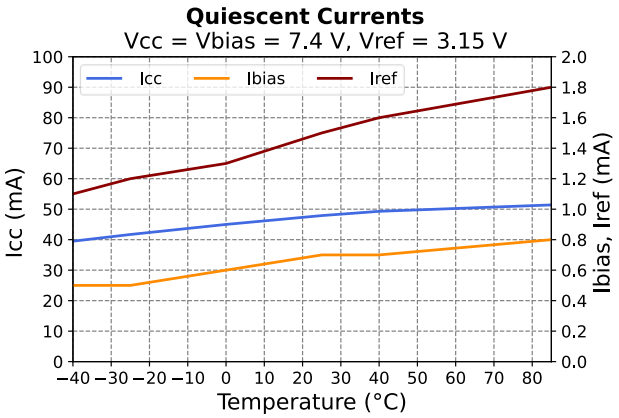


Figure 37 - Idle Currents vs. Temp

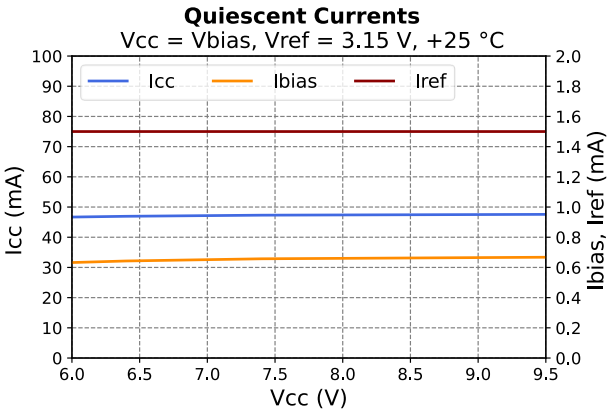


Figure 38 - Idle Currents vs. Vcc

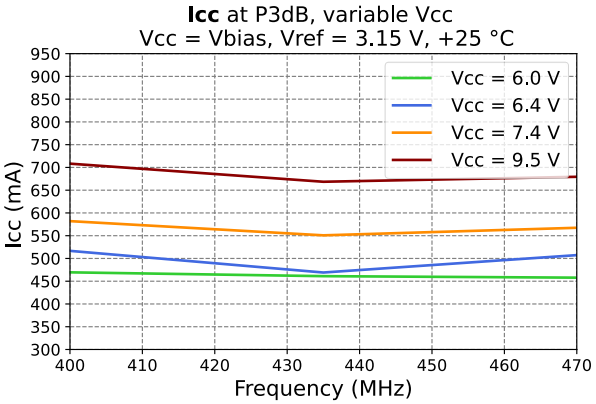


Figure 39 - Icc at P3dB

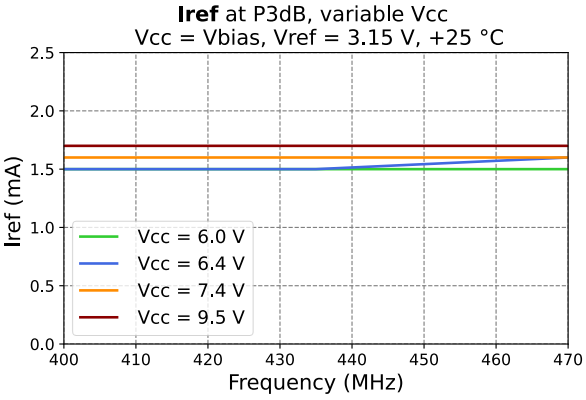


Figure 40 - Iref at P3dB

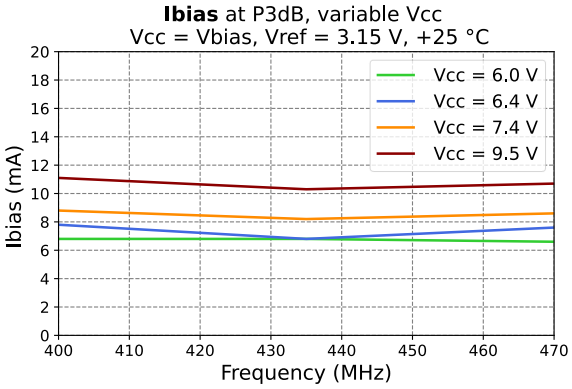


Figure 41 - Ibias at P3dB

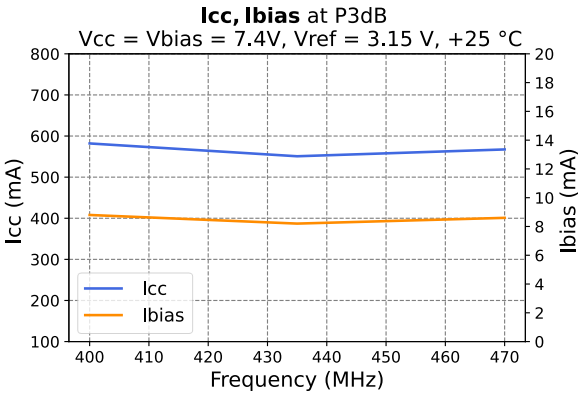


Figure 42 - Icc and Ibias at P3dB

Test conditions unless otherwise noted:-
Vcc = Vbias = +7.4 V, Vref = Vref1 = Vref2 = +3.15 V, Ta = +25 °C, Zo = 50 Ω.

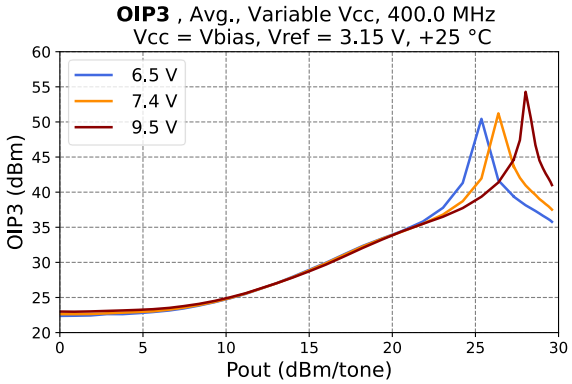


Figure 43 - OIP3 vs. Pout at 400 MHz

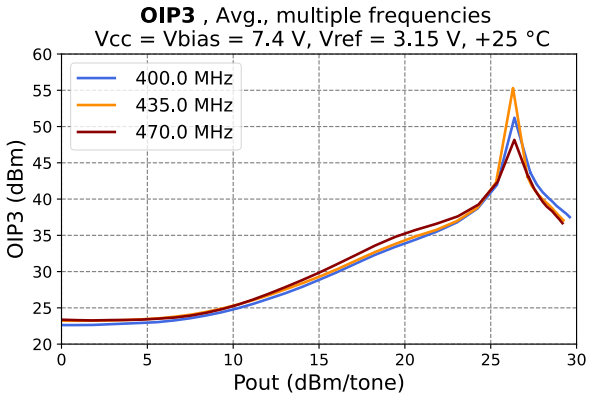


Figure 44 - OIP3 vs. Pout

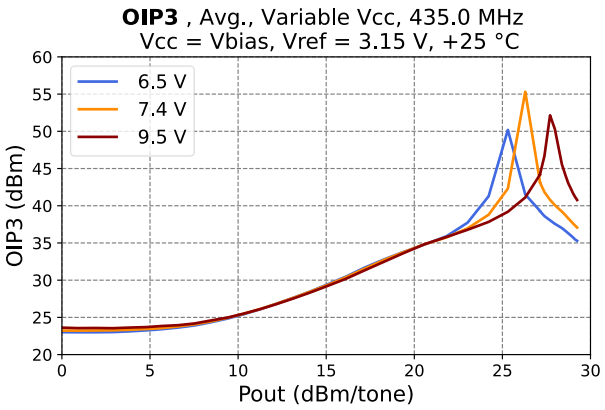


Figure 45 - OIP3 vs. Pout at 435 MHz

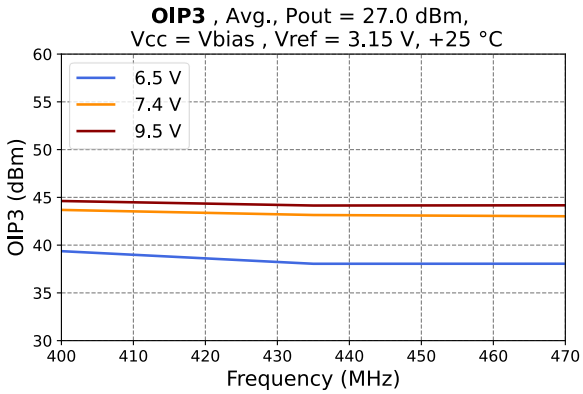


Figure 46 - OIP3 vs. Frequency at Pout = 27 dBm/tone

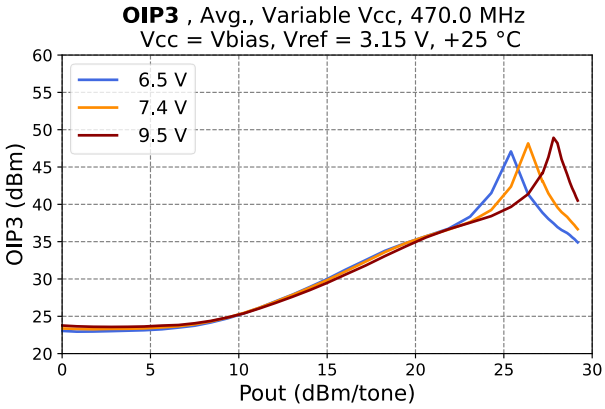


Figure 47 - OIP3 vs. Pout at 470 MHz

Test conditions unless otherwise noted:-
Vcc = Vbias = +7.4 V, Vref = Vref1 = Vref2 = +3.15 V, Ta = +25 °C, Zo = 50 Ω.

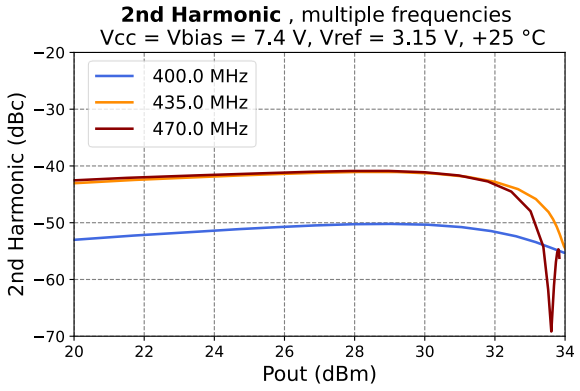


Figure 48 - Second Harmonic vs. Pout

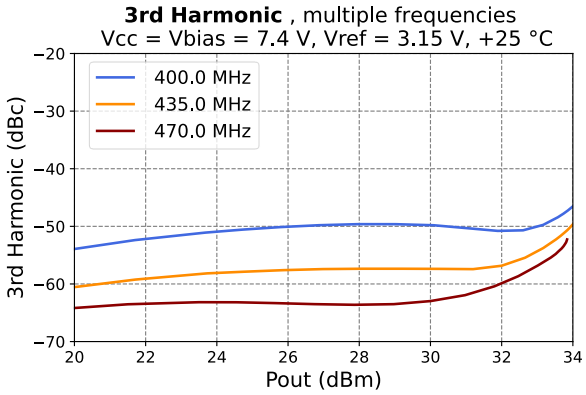


Figure 49 - Third Harmonic vs. Pout

Application Information

Evaluation Board Schematic

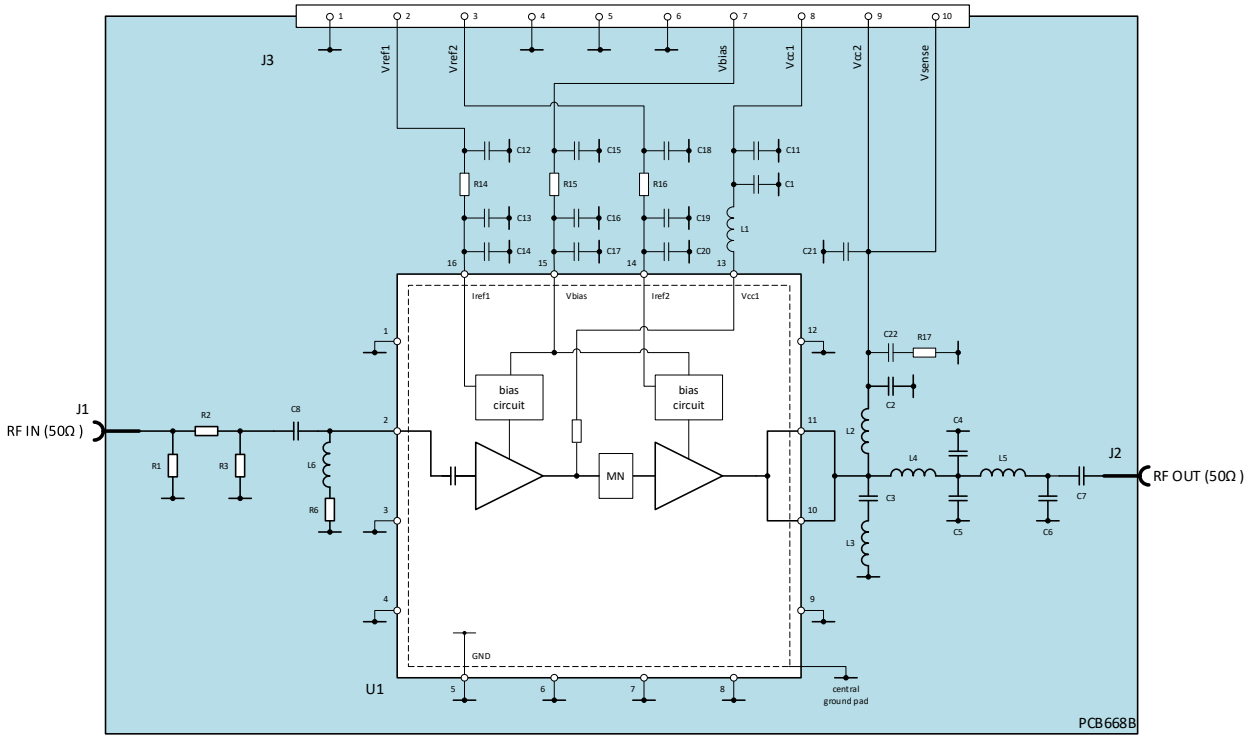


Figure 50 - EV90A007 Schematic

Bill Of Materials (BOM)

The following BOM is for the 400 to 470 MHz operating band, contact CML for BOM details for other operating bands.

Reference Designator	Value	Size	Description
C1	220 pF	0603	COG, 50 V, +/-5 %
C7	220pF	0402	C0G, 100 V, +/- 5%
C2	120 pF	0603	COG, 50 V, +/-5%
C8	10 pF	0402	COG, 50 V, +/-1%
C3, C5	8.2 pF	0603	COG, 100 V, +/-0.1pF
C4	9.1 pF	0603	COG, 100 V, +/-0.1pF
C6	6.2 pF	0603	COG, 100 V, +/-0.1pF
C14, C17, C20, C22	100 nF	0402	X7R, 50 V, +/-5 %
C11, C16	1 uF	0603	X7R, 50 V, +/-10 %
C12, C13, C15, C18, C19	DNF	0603	
C21	10 uF	TANT_A	TANT, 25 V, +/-20 %
L1	27 nH	0603	Coilcraft: 0603DC-27NXGR, +/-2%
L2	33 nH	0603	Coilcraft: 0603AF-33NXJR, +/-5%
L3	3.3 nH	0603	Coilcraft: 0603CS-3N3XGR, +/-2%
L4	6.2 nH	0603	Coilcraft: 0603DC-6N2XGR, +/-2%
L5	12 nH	0603	Coilcraft: 0603DC-12NXGR, +/-2%
L6	16 nH	0402	Coilcraft: 0402DC-16NXGR, +/-2%
R2	0 R	0402	0.063 W, +/-1%
R6	22 R	0402	0.063 W, +/-1%
R14, R16	732 R	0402	0.063 W, +/-1%
R15	100 R	0603	0.1 W, +/-1%
R17	5.1 R	0402	0.1 W, +/-1%
R1, R3	DNF	0402	
U1	CMX90A007Q7		
J3	10-way 0.1” pin header (TE 1-640456-0, mating 4-640440-0)		
J1, J2	Molex: 73251-1150		

Note: DNF = Do Not Fit

Use of alternative component tolerances, voltage rating, types or manufacturers may result in lower performance.

PCB Layout

Careful layout of the printed circuit board (PCB) is essential for stable RF and good thermal performance. The recommended layout, including the ground via pattern underneath the device, may be taken from the evaluation board (Part Number EV90A007). See the following section for recommendations on best thermal and RF design.

The PCB consists of four-layer FR-4 with a total thickness of 1.592 mm (Figure 51) and the EV90A007 PCB (Figure 52) is 50 mm x 50 mm. The microstrip 50 Ω RF input and output width is 0.38 mm.

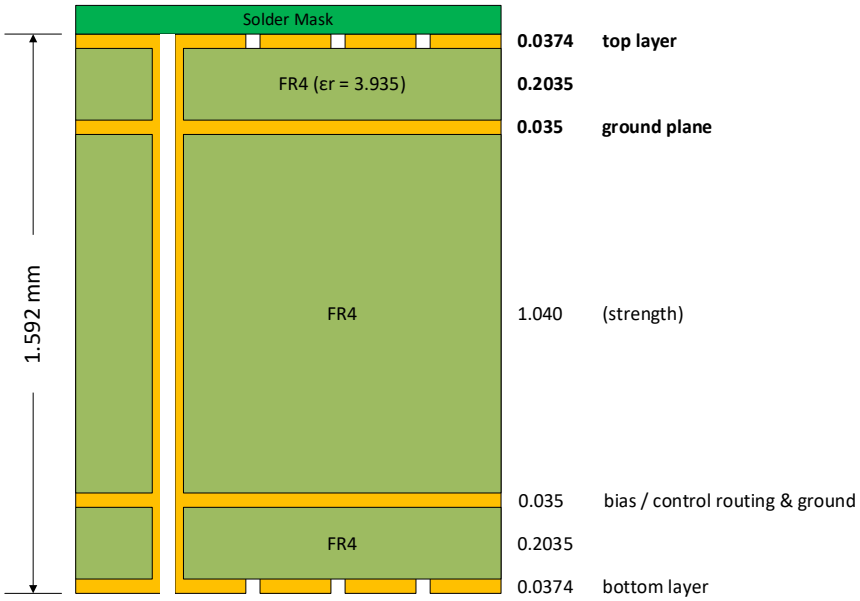


Figure 51 - EV90A007 PCB Layer Stack

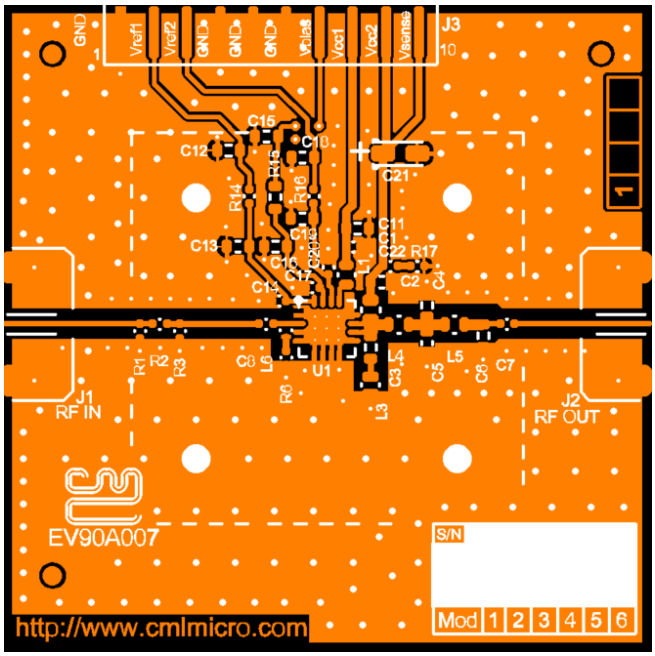


Figure 52 - EV90A007 PCB Top Layer View

Thermal and Stability Design

The primary RF/DC ground and thermal path is via the exposed die pad on the backside of the package, which must be connected to the PCB ground plane. An array of plated through-hole vias directly underneath the die pad area is essential to conduct heat away and minimise ground inductance. A typical solution should have 9 grounding vias connecting the top layer to the bottom layer, with inner diameter of 0.2 mm (and 0.025 mm plating) on a 0.9 mm grid pattern. The vias do not need to be filled. The PCB layout should provide a thermal radiator appropriate for the intended operation, adding as much copper to inner and outer layers as possible to avoid excessive junction temperature.

Device junction temperature (Tj) can be calculated using Tj = Tc + (Pdiss x Rjc) where Pdiss = Pdc + Pin - Pout and Tc is the case temperature on the backside of the package (die pad) in contact with the PCB.

A heatsink should be used if the thermal performance of the PCB layout is not adequate and particularly if the user is running the device continuous at high output power. The heatsink should be attached to the rear of the PCB using mounting screws positioned close to the device to ensure good contact with the ground via pattern. The backside of the PCB is clear of solder resist to enable a heatsink to be applied and it is recommended to use thermal grease to ensure good contact between the PCB and the heatsink.

A low inductance connection as described between the central ground pad and the board RF ground plane prevents unwanted gain peaking and instability due to internal ground path feedback.

RFin Matching

The CMX90A007 RFin (pin 2) requires external matching to 50 Ω. There is provision for a Pi attenuator at R1, R2 and R3. At 435 MHz, the target impedance to present to RFin is 40 + j15 Ω to meet the 400 to 470 MHz operating characteristics (Vcc = Vbias = +7.4 V, Vref = +3.15 V). The EV90A007 evaluation board uses two sections to achieve this. In the DC block section, C8 acts as a DC block to protect devices connected to J1 but also moves the impedance. The shunt LR section (L6 and R6) transforms this impedance to present the target impedance to the CMX90A007 RFin and assists with gain flatness and stability at lower frequencies. At these frequencies the interconnecting track and ground via paths need to be considered as part of any initial simulation. Some adjustment of values may be needed in a final layout to achieve optimal performance.

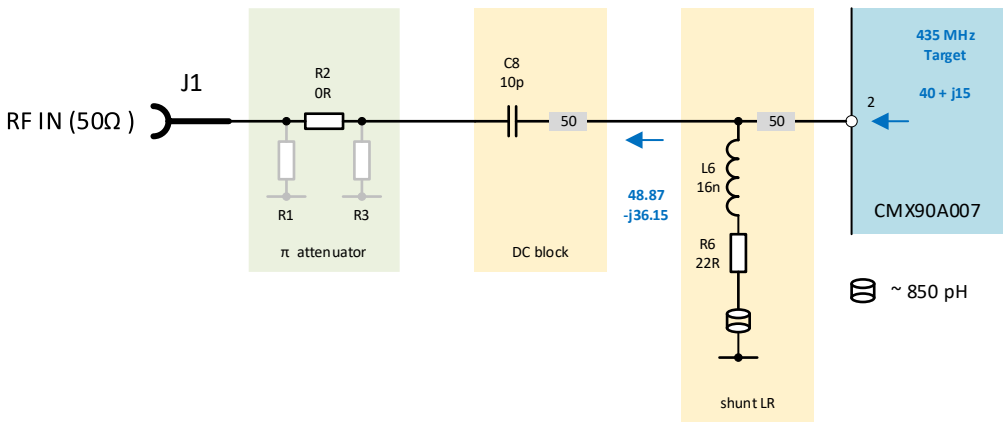


Figure 53 – Diagram of the EV90A007 Input Matching Network including inductance of vias and track impedances

RFout Matching

The RFout (pins 10 & 11) require matching to 50 Ω. At 400 to 470 MHz, along with a suitable external inductor (L2) for the Vcc supply. This must be capable of carrying the dc current under all operating conditions and associated RF decoupling on the supply side is required. At 435 MHz, the target impedance the matching circuit should present to

the device is ~13.3 Ω to meet the 400 to 470 MHz operating characteristics (Vcc = Vbias = +7.4 V, Vref1 & Vref2 = +3.15 V). The matching network on EV90A007 consists of four sections that present this impedance to the device from 50 Ω. C7 acts as a DC block to protect devices connected to J2. The MS1 section (C6 shunt capacitor and L5 series inductor) transforms this impedance to an intermediate point on the real axis close to the geometric mean. Section MS2 (C4/C5 shunt capacitors and series inductor) brings the impedance close to the target impedance for the CMX90A007 RFout. MS3 includes the Vcc feed inductor and the 2nd harmonic short required for improved efficiency and the connecting transmission line to the two output pins. The Vcc feed is inductive, and the harmonic trap is capacitive at 435 MHz and, with the final transmission line, act as the final matching network to present the target impedance to the CMX90A007 RFout. At these frequencies and impedances, the interconnecting track and ground via paths need to be considered as part of any initial simulation. Some adjustment of values may be needed in a final layout to achieve the specified performance.

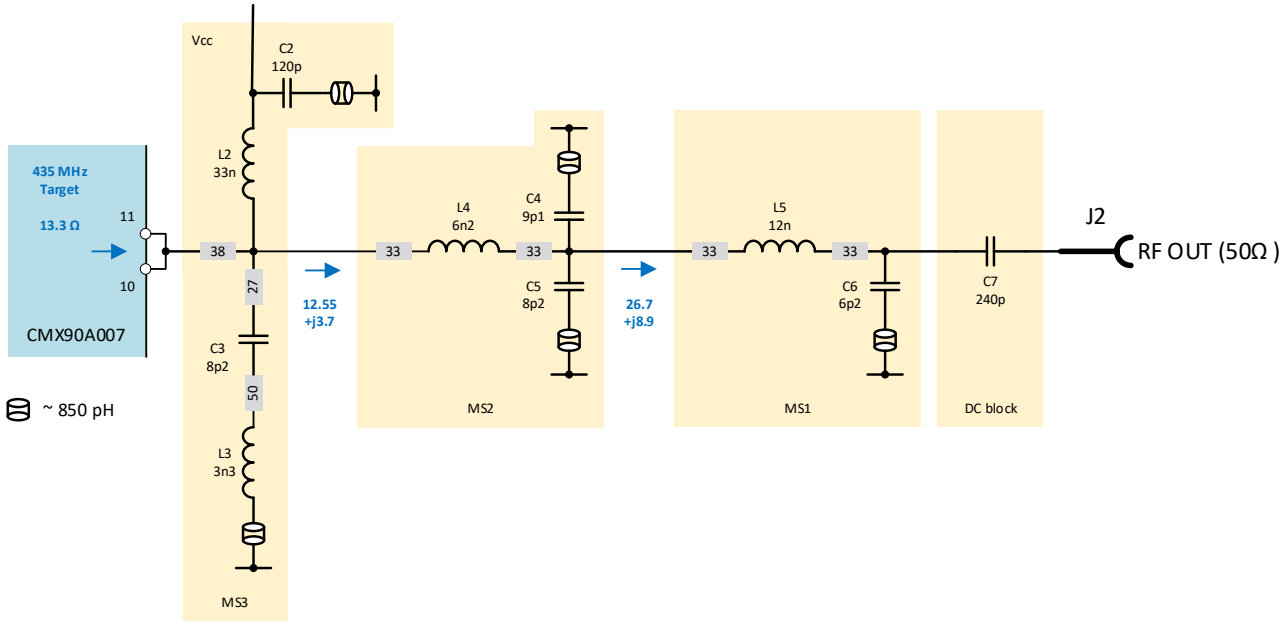


Figure 54 – Diagram of the EV90A007 Output Matching Network including inductance of vias and track impedances

Vcc1 & Vcc2 Pins

Vcc1 provides the collector supply to stage 1 with external RF choke (L1) and decoupling. The optimum value of choke and decoupling will vary with frequency band. Vcc2 is common with RFout and requires an external RF choke to provide a low resistance path for the collector supply to stage 2. An external inductor (L2) capable of carrying the DC current under all operating conditions and associated RF decoupling is required. No internal ESD protection is used on these pins as the RF performance would be compromised by the associated parasitics.

Vbias Pin

The Vbias pin provides the supply to the internal bias circuits and the associated base currents to the two amplifier stages. To consolidate power supplies the Vbias pin can be connected to the Vcc pins at the supply input without affecting the performance of the device. This pin is protected by ESD diodes.

Iref1 & Iref2 Pins

The quiescent bias current of each stage is proportional to the current into the associated Iref pin. This current is set by a series resistor from the Vref regulated supply. These resistors are 732 Ω (R14, Iref1) and 732 Ω (R16, Iref2) on the EV90A007, resulting in the following currents with Vref = 3.15 V:

Iref1 = (Vref – (2 x Vbe)) / (R14 + Rint)

Current into Iref1 = (3.15 – (2 x 1.25)) / (732 + 134) = 0.75 mA, resulting in a typical Icq1 of 9.9 mA.

Icq1 (approx.) = (Iref1 x 9.9/0.75) – ((Iref – 0.75) x 11.5)

Iref2 = (Vref – (2 x Vbe)) / (R16 + Rint)
Current into Iref2 = (3.15 – (2 x 1.25)) / (732 + 134) = 0.75 mA, resulting in a typical Icq2 of 39.6 mA.
Icq2 (approx.) = (Iref2 x 39.6/0.75) – ((Iref – 0.75) x 11.5)

These bias points have been selected for optimum PA performance. It is possible to achieve these same currents from higher or lower Vref supplies by appropriate selection of the series resistors. To ensure correct bias circuit operation the current into either Iref1 or Iref2 should not exceed 3.5 mA. These pins are protected by ESD diodes.

Ramping

Vref1 and Vref2 can also be used to ramp the CMX90A007 gain up or down to support burst signals and TDD systems. By varying Vref1 and 2 together between 2 V and 3.15 V (typ.) the gain can be adjusted by 80 dB (Figure 55).

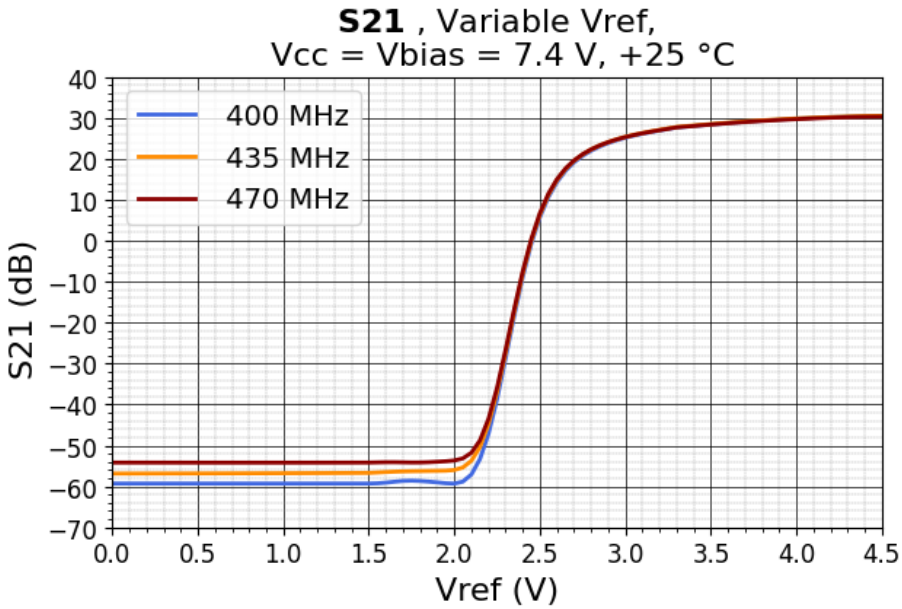


Figure 55 – Vref Gain Control

Evaluation Board and Bias Procedure

Ensure an adequately rated attenuator is placed between the output of the amplifier (RFout) and 50 Ω RF test equipment. The amplifier RFin should be connected to a signal generator with RF OFF. A dual power supply will be needed, with output of +7.4 V @ 2 A for the collector voltages (Vcc = Vcc1 and Vcc2) and bias circuit (Vbias) and +3.15 V for the reference voltages (Vref1, Vref2). Use good quality cables to minimise the voltage drop between the PSU and evaluation board, particularly for Vcc2. A Vsense pin (10) is provided on the board to optionally enable feedback to a suitably equipped power supply to compensate for the cable voltage drop at high current. This is connected in parallel with Vcc2. Connect the power supply with RF off and ensure that the evaluation board consumes the correct quiescent current (Icq). Although it is good practice to enable the Vcc & Vbias supply before the Vref supplies, in general, power supply sequencing is not necessary. If the quiescent current is correct, enable the RF signal with a low level, for example RFin = -30 dBm to begin with, to ensure the device is not overdriven. Ensure the test signal is within the recommended frequency range of the device and that the output signal measured on the test equipment complies with the expected small signal gain, before continuing with any further tests.

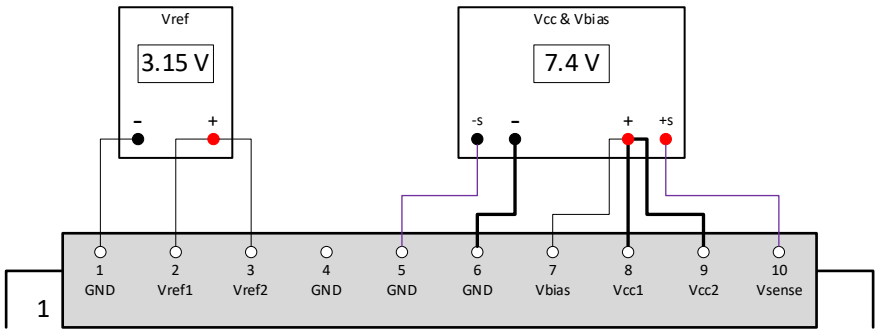


Figure 56 – EV90A007 Standard Power Supply Connections: common Vcc & Vbias PSU

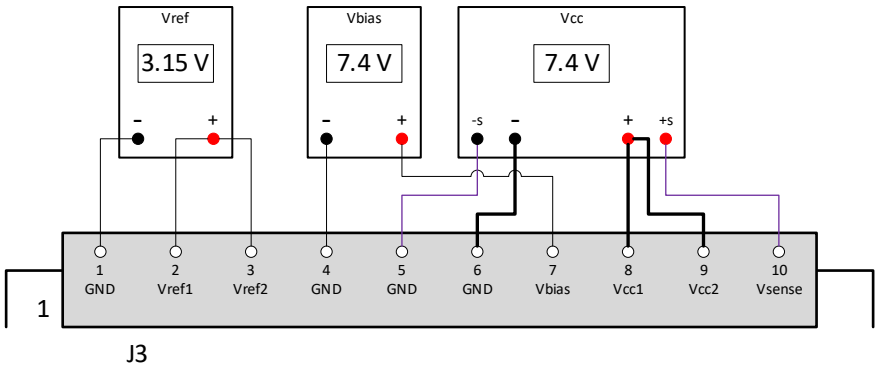


Figure 57 – Alternative EV90A007 Power Supply Connections: separate Vcc & Vbias PSUs

The user should be aware that noise from power supplies may modulate the amplified RF signal and introduce spurious products in the output spectrum. Ensure that the power supplies used are 'RF quiet'.

Ruggedness

To prevent possible damage to the device, care should be taken to ensure that the VSWR of the load that the CMX90A007 is working into does not exceed the limits in the Electrical Specification.

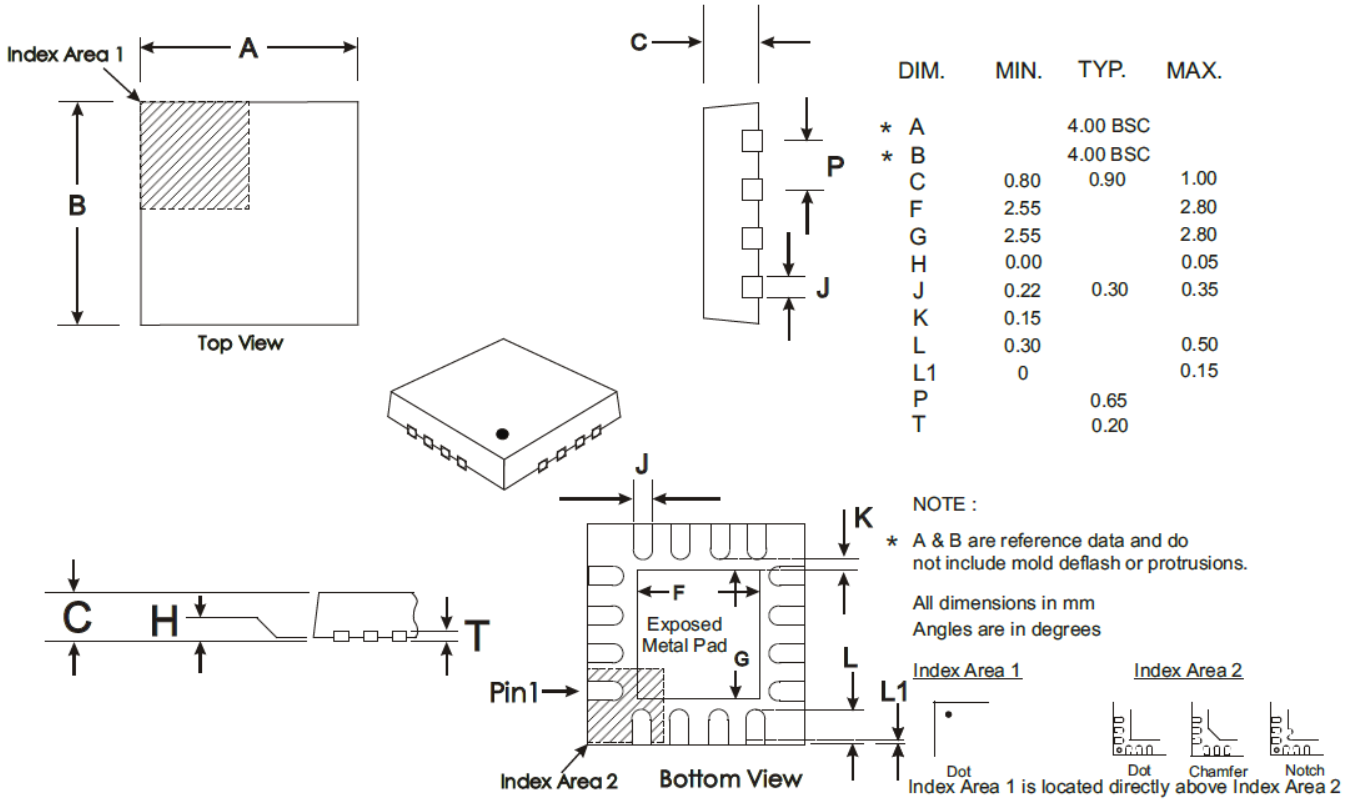
A typical transmit system will have couplers, filtering, transmit/receive switching and antenna matching between the PA and the antenna. These all need to be designed carefully to ensure a good 50 Ω match is presented to the PA that is above the minimum return loss limits over the whole operating frequency range.

External effects on the antenna impedance should also be considered. Proximity to other objects and surfaces can change the antenna impedance significantly, resulting in the return loss presented to the PA falling below the limit and therefore subsequent damage to the PA.

If there is an external antenna connector on the equipment, it should be assumed that the wrong antenna might get connected or that the transmitter may be operated with no antenna connected.

Package Outline

16-lead 4x4mm VQFN Package (Q7)



DIM.	MIN.	TYP.	MAX.
* A		4.00 BSC	
* B		4.00 BSC	
C	0.80	0.90	1.00
F	2.55		2.80
G	2.55		2.80
H	0.00		0.05
J	0.22	0.30	0.35
K	0.15		
L	0.30		0.50
L1	0		0.15
P		0.65	
T		0.20	

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

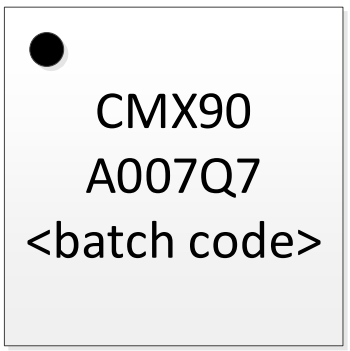
All dimensions in mm
Angles are in degrees

Index Area 1 is located directly above Index Area 2

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Package Marking

Pin 1 indicator (dot) and 3 rows of text for device identification.



Line 1: CMX90 SµRF series

Line 2: 6-character part code

Line 3: Batch code

Revision History

Issue	Description	Date
1.0	First approved release	21st March 2025

Contact Information

For further information please contact your local CML sales representative.

Contact details can be found at www.cmlmicro.com