

Features

- Frequency Range: 13-15.5GHz
- Pout: 45.5 dBm @ 21dBm Pin
- PAE: >32 %
- Small Signal Gain: 24dB
- Bias: VD=28V IDQ=350mA
- Technology: GaN-on-SiC
- Lead-free and RoHS compliant
- Die Size: 3.6mm x 4.4mm

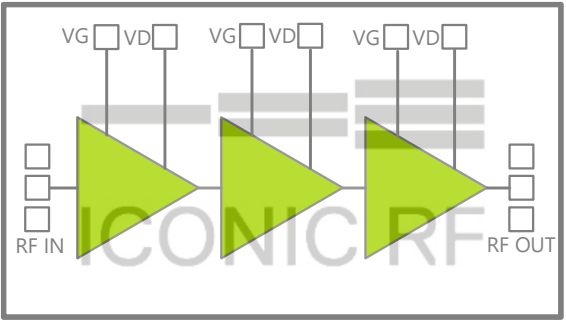
Applications

- Satellite Communications
- Aerospace & Defense

Description

The ICP1445 is a three stage MMIC power amplifier in bare die form, fabricated using GaN-on-SiC technology. ICP1445 operates from 13-15.5GHz with 45.5dBm output power, >32% PAE and 24dB small signal gain. The ICP1445 is well suited for a wide variety of commercial and defense applications. The RF input and output ports have integrated DC blocking capacitors and are matched to 50 Ohm impedances.

Functional Diagram



Electrical Specifications | Test Conditions unless otherwise stated | $V_D=28V$, Pulse Period 1ms, Duty Cycle 10%

Parameter	Units	Min.	Typ.	Max.
Frequency	GHz	13		15.5
Output Power P_{sat} @ $P_{in}=26dBm$	dBm		45.5	
PAE @ P_{sat} $P_{in}=26dBm$	%		32	
Saturated Gain $P_{in}=26dBm$	dB		19	
Small Signal Gain	dB		24	
Input Return Loss	dB		15	
Output Return Loss	dB		7	
Quiescent Current	mA		350	

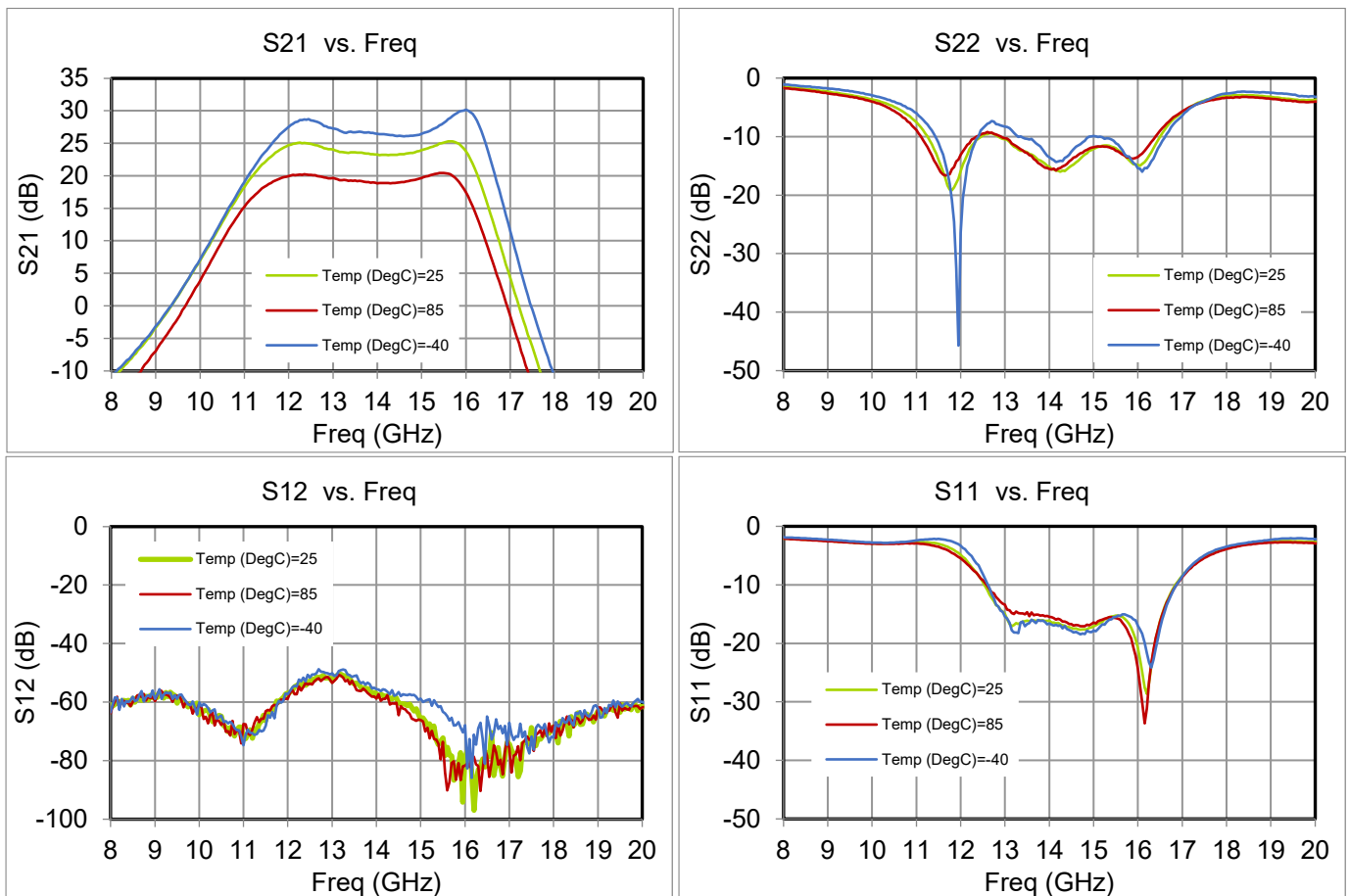
Absolute Maximum Ratings

Parameter	Absolute Maximum
Drain Voltage (V_{DG})	32V
Gate Voltage Range (VG)	-5 to 0V
Drain Current (CW) $T_A=25^\circ\text{C}$	6A
Power Dissipation (CW) $T_A=25^\circ\text{C}$	200W
Power Dissipation (CW) $T_A=85^\circ\text{C}$	140W
CW Input Power	+33dBm
Input Power (Pulsed 10%) VSWR (3:1), $V_D=28\text{V}$, $I_{DQ}=350\text{mA}$	+30dBm
Channel Temperature	275°C
Storage Temperature	-65°C to $+150^\circ\text{C}$

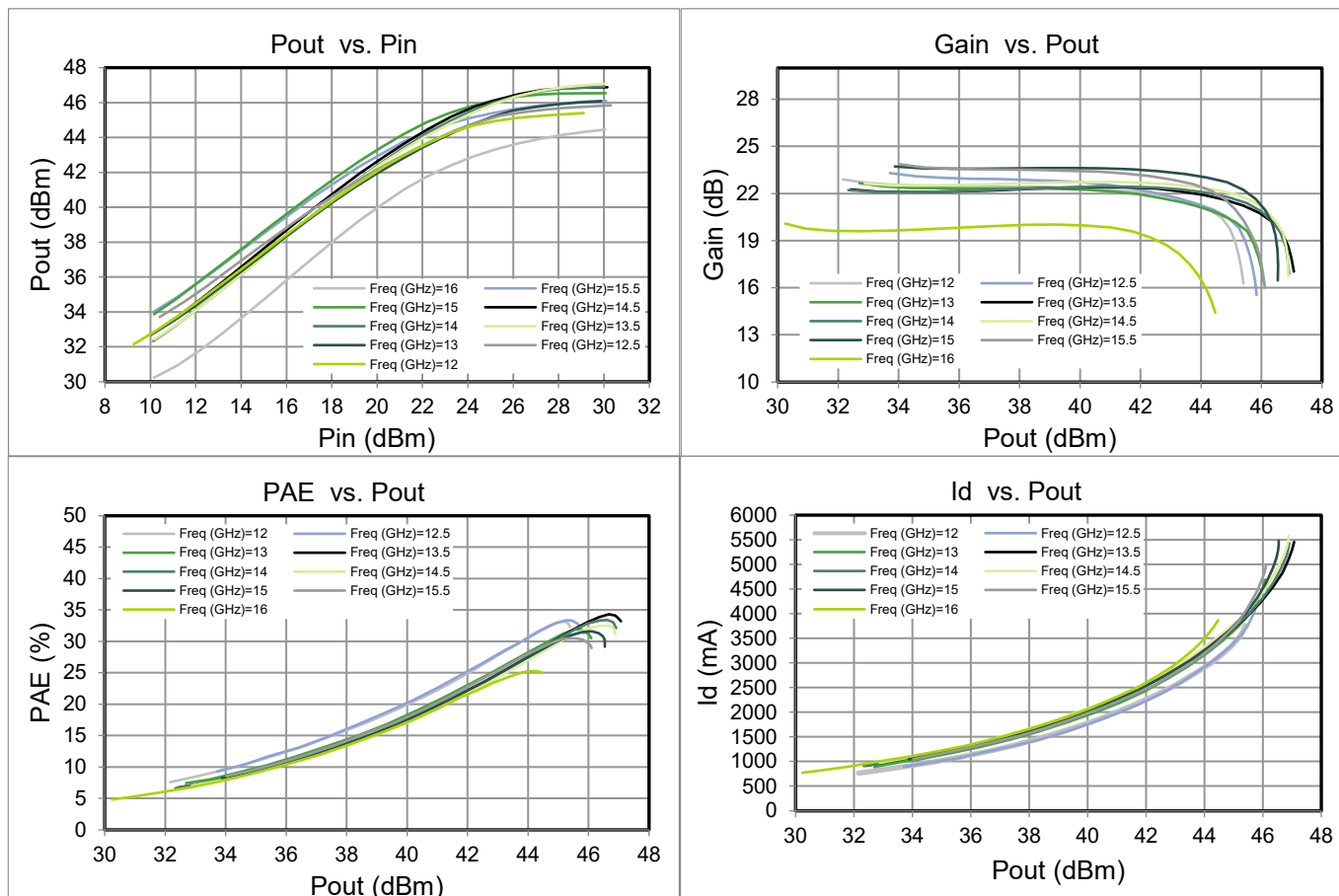
Exceeding any one or combination of these limits may cause permanent damage to this device.
Microchip Technology does not recommend sustained operation near these survivability limits.

Typical Performance

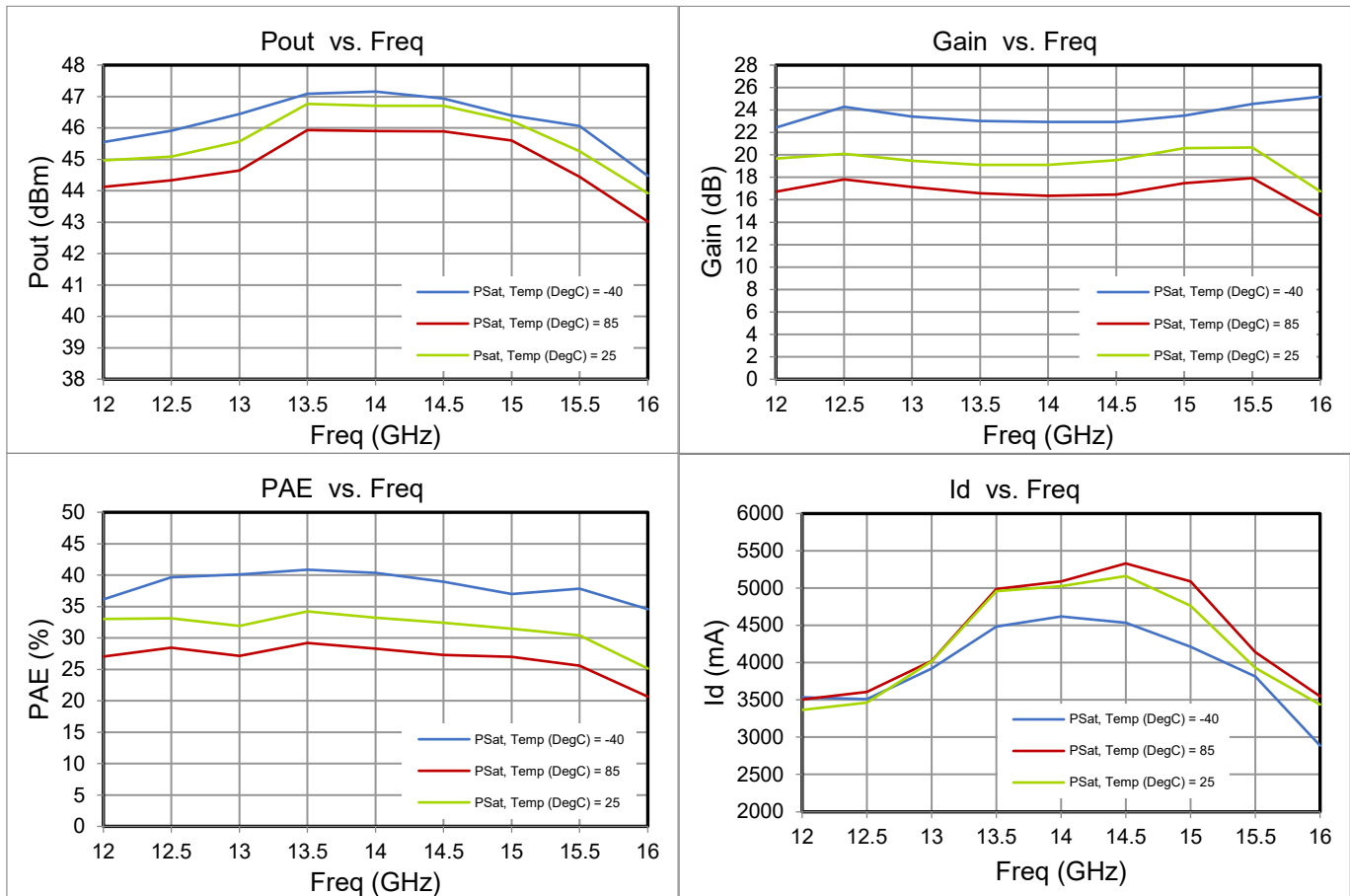
S-Parameter Performance | Test Conditions unless otherwise stated | $V_D=28\text{V}$, $I_D=350\text{mA}$, $T_A=25^\circ\text{C}$



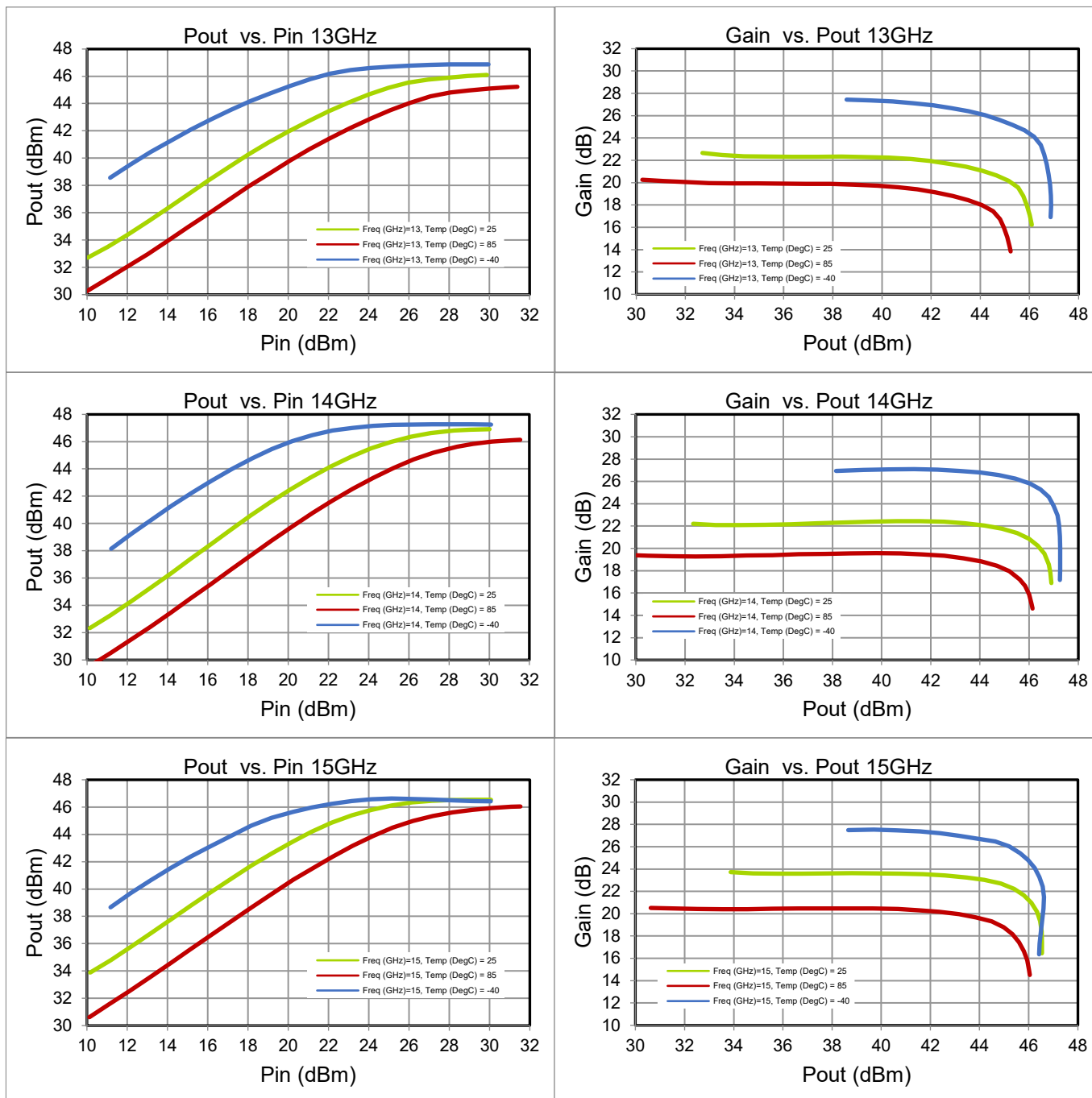
Power Performance | Test Conditions unless otherwise stated | $V_D=28V$, $I_D=350mA$, $T_A=25^\circ C$, Pulse Period 1ms, Duty Cycle 10%



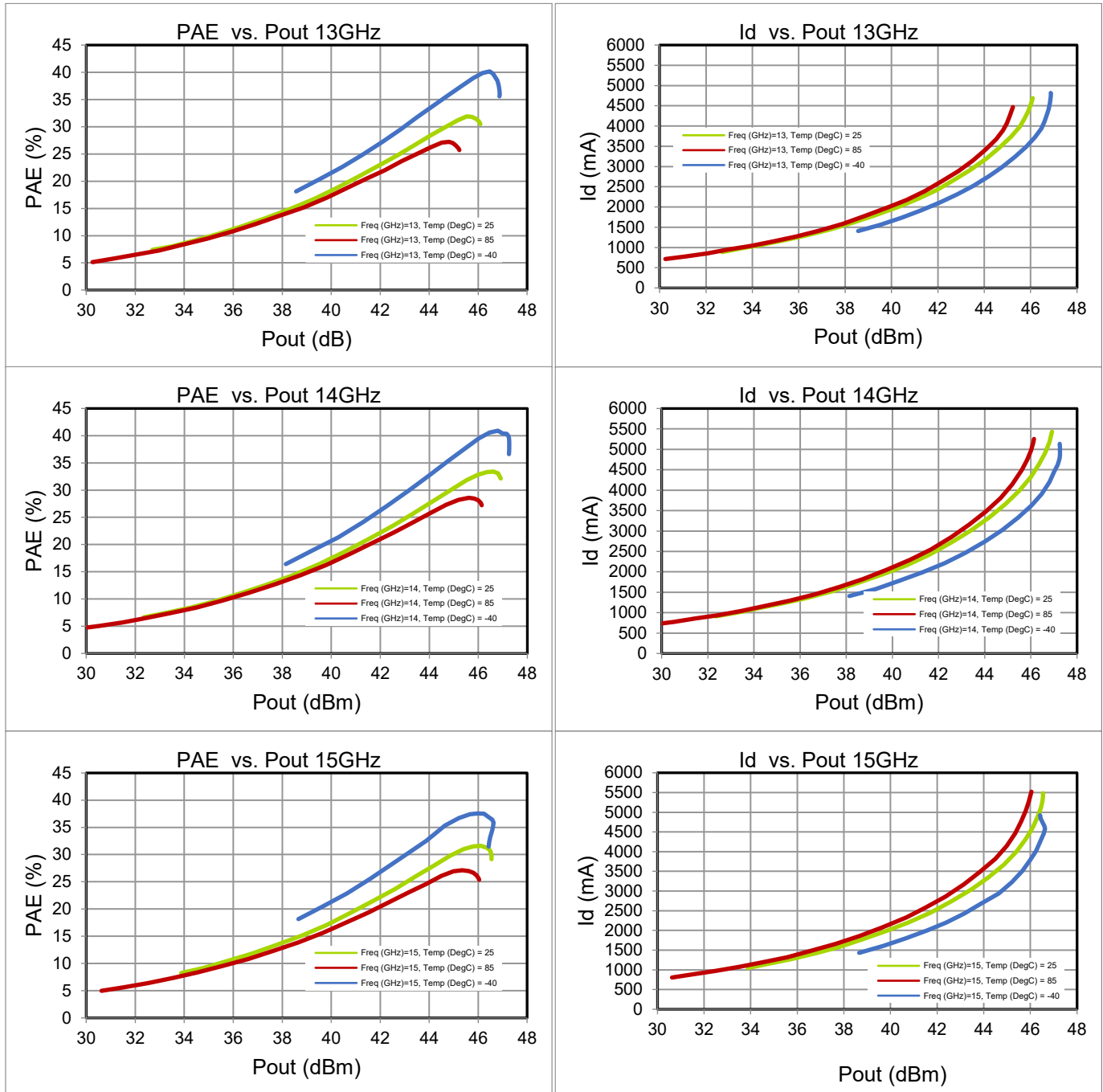
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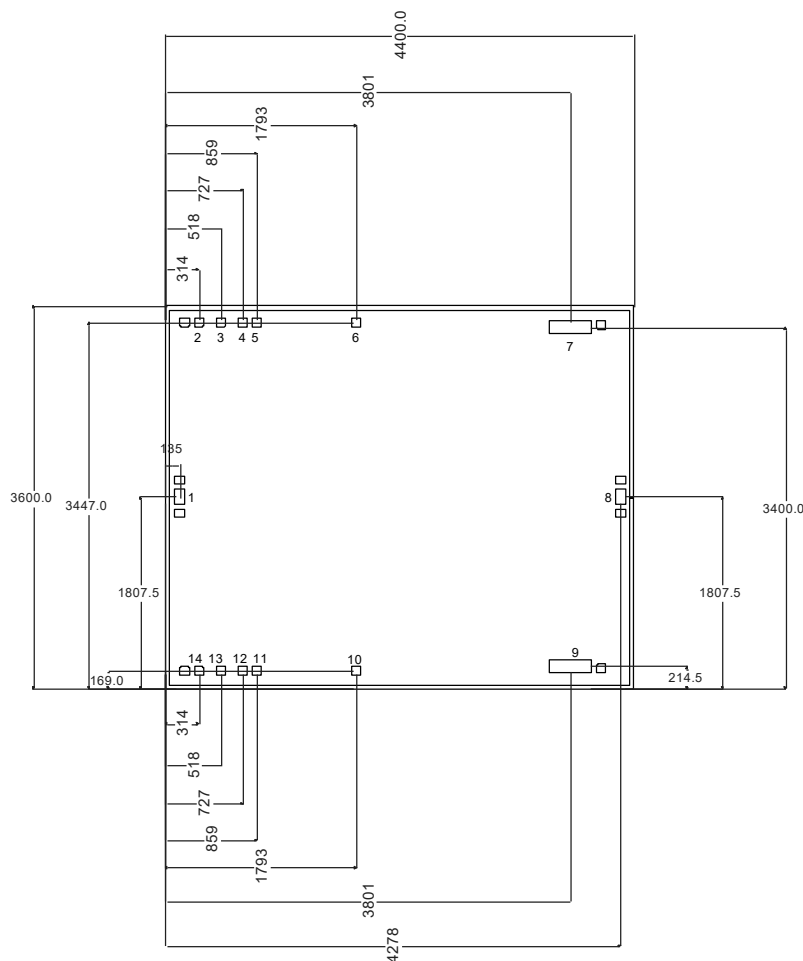
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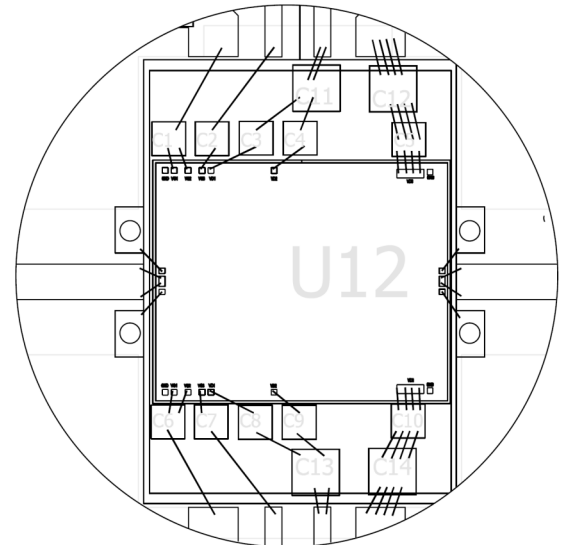
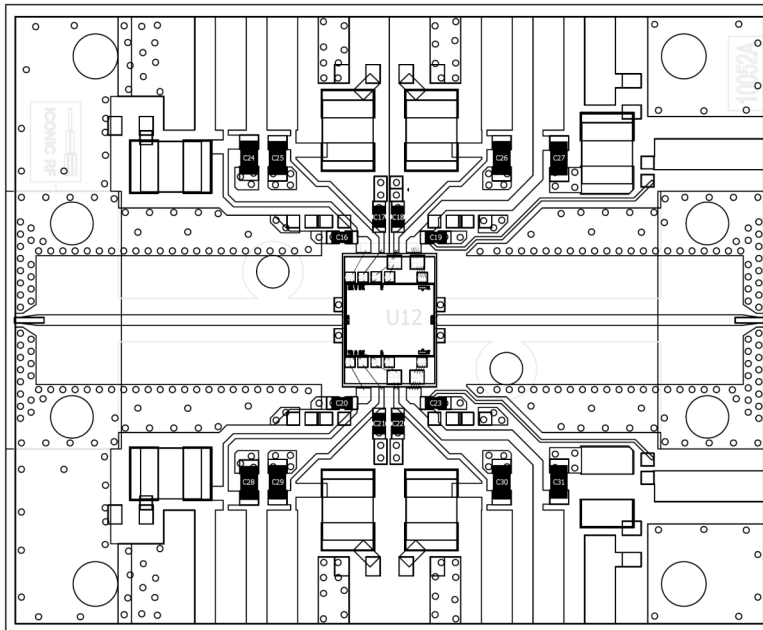


Mechanical Drawing



Units: um
Thickness: 0.1mm
Backside of Chip is RF and DC

Pad No	Pad Size (um)	Function	Description
1	89 x 150	RFIN	50 Ohm RF input, DC blocked
2,14	85 x 85	VG1	First stage gate bias, decoupling and bypass caps required
3,13	85 x 85	VG2	Second stage gate bias, decoupling and bypass caps required
4,12	85 x 85	VG3	Third stage gate bias, decoupling and bypass caps required
5,11	85 x 85	VD1	First stage drain voltage, decoupling and bypass caps required
6,10	85 x 85	VD2	Second stage drain voltage, decoupling and bypass caps required
7,9	130 x 400	VD3	Third stage drain voltage, decoupling and bypass caps required, must be biased from both sides
8	89 x 150	RFOUT	50 Ohm RF output, DC blocked, pad is DC grounded



DETAIL A - BONDING
SCALE 5 : 1

Bill of Materials

Assembly Reference	Value	Description	Manufacturer Part No.
U12		ICP1445 MMIC	ICP1445
C1-C10	100pF	SLC Capacitor	Johanson 500U01A101MT4W
C11-C14	10000pF	SLC Capacitor	Knowles V30BZ103M1SX
C16-C23	10nF	0402 size Capacitors	Various
C24-C31	10uF	0603 size Capacitors	Various

Assembly Guidance

Amplifier must be biased from both sides.
Optimum RF power performance achieved by minimizing output RF bond wire length.

Interconnect assembly Notes

- Ball Bonding is preferred technique
- Force, time and ultrasonic parameters are critical.
- Aluminum wire bonding is not recommended.
- Bond Wire diameter of 1mil is recommended.

Die attach of component using adhesive

- Vacuum collets are preferred method of pickup.
- Pickup method must consider the avoidance of die air bridges.
- Die suitable for Eutectic and Epoxy die attach.

- Where Epoxy is used, high thermal conductivity Silver Sintered Epoxy is recommended:-

- Namics H9889-1

Reflow Process

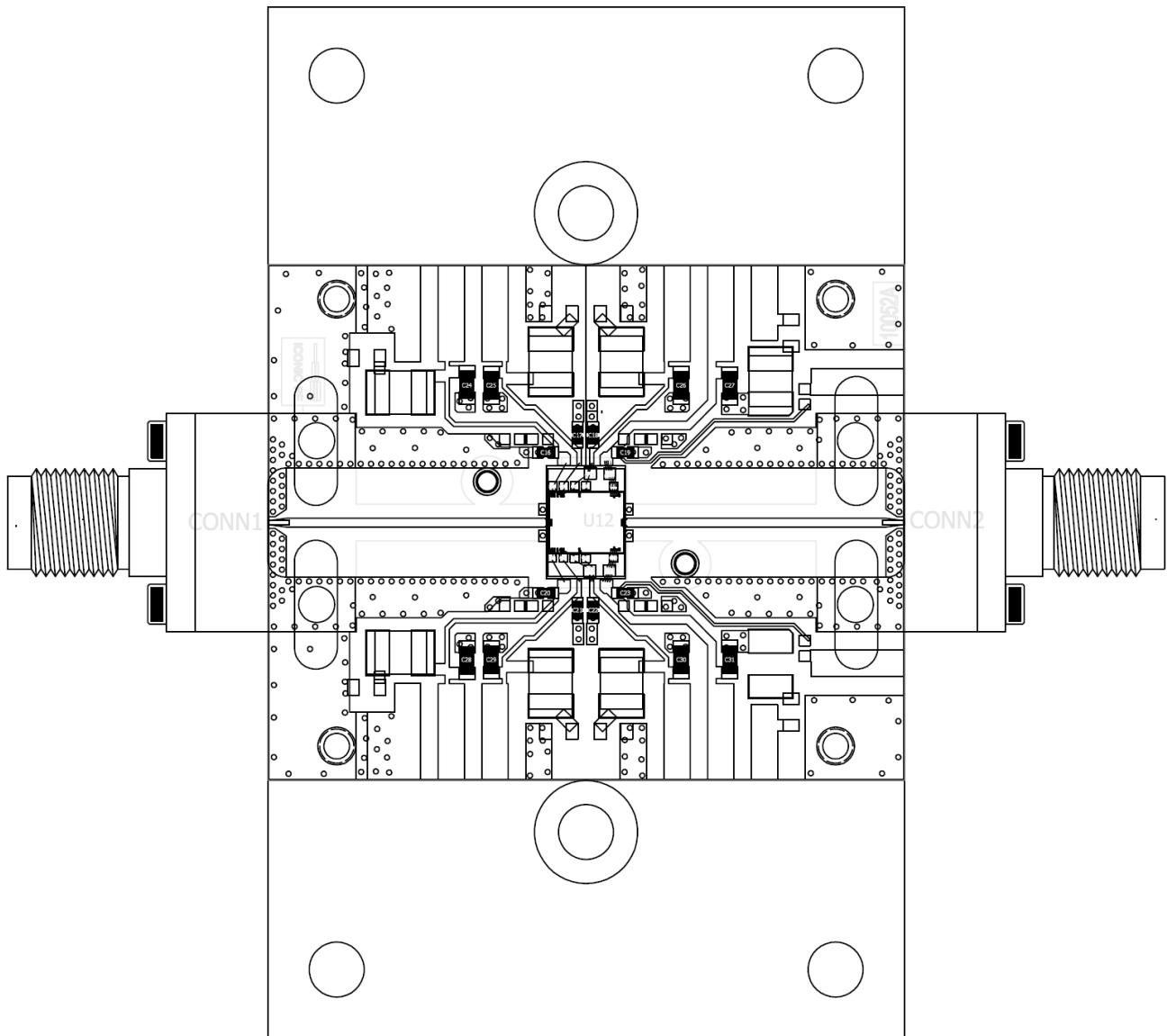
- Maximum temperature 320°C for 30 seconds.
- Material matching for coefficient of thermal expansion is crucial for long-term reliability

Assembly Guidance continued:

For optimum RF and thermal performance Microchip Technology recommends the die assembly base plate is adequately bolted to a forced air heat sink using a thermal graphite interface pad (Graphite Interface Material GCSP-017-G 170 μ m thick).

There are many variables of the second level assembly between the die base plate and heat sink that Microchip Technology is unable to control, and the following guidance is provided as information only. Fixing bolts should be provided as close to the die as possible to ensure an optimum pressure between the base plate and the heat sink.

The bolting screws used to attach the PCB assembly to the heat sink must include washers and be tightened with a suitable tightening pattern to ensure a uniform pressure. It is advised all surfaces be cleaned and be free of grease and dust prior to fully aligning the assembly with all screws located and tightened to finger tight. Further torquing of the screws must be achieved in multiple phases using a star shaped pattern to a recommended torque of 2.5 N/m.



Bias-Up Procedure

1. Set $V_G = -5V$
2. Set V_D to 28V
3. Adjust V_G positive until I_D quiescent is 350mA
4. Limit I_D to 2A
5. Apply RF Signal

Bias-down Procedure

1. Turn off RF
2. Turn off V_D , allow drain capacitor to discharge
3. Turn off V_G .

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices. Class 1A HBM (250-500V) ESD Classification is anticipated.

