MICROCHIP

Vectron™ Oscillators

VCC1A

CMOS Crystal Oscillator

Description

Vectron's VCC1A Crystal Oscillator (XO) is a quartz stabilized square wave generator with a CMOS output. The VCC1A uses a fundamental or 3rd overtone crystal resulting in very low jitter performance, and a monolithic IC which improves reliability and reduces cost.

Features

- Ultra Low Jitter, Fundamental or 3rd OT Crystal Design
- CMOS Output Crystal Oscillator
- Output Frequencies from 1.024 MHz to 160.000 MHz
- +1.8, +2.5, +3.3 or +5.0V Operation
- Output Disable Feature
- Excellent ±25ppm temperature stability
- -10/70 - 55/125°C operating temperature options
- Small Industry Standard Package, 7 x 5 mm
- Product is compliant to RoHS directive and fully compatible with lead free assembly (Excluding solder dipped, _SNPB, option)

Applications

- SONET/SDH/DWDM
- Ethernet, GE, SynchE
- Storage Area Networking
- Fiber Channel
- Digital Video
- Broadband Access
- Base Stations, Picocells
- Driving A/D's, D/A's, FPGA's
- Test and Measurement
- COTS

Block Diagram

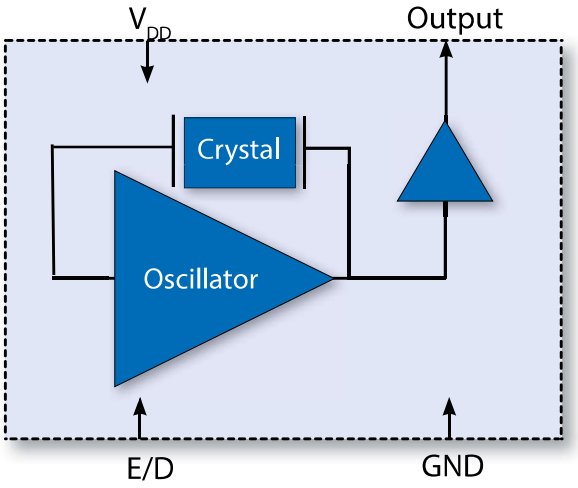


Table 1. Electrical Performance, 5V Option					
Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply					
Voltage[1]	V_{DD}	4.5	5.0	5.5	V
Max Supply Voltage Max Voltage E/D		-0.5 -0.5		7.0 V_{DD}+0.5	V V
Current[2,] ≤12MHz 12.001-20MHz 24.001- 65MHz 65.001-100Hz	I_{DD}			 5 13 21 30	mA
Current, Output Disabled				10	uA
Frequency					
Nominal Frequency	f_N	1.024		100.000	MHz
Stability[4], (Ordering Option)		±25, ±32, ±50, ±100			ppm
Outputs					
Output Logic Levels[2] Output Logic High Output Logic Low	 V_{OH} V_{OL}	 0.9*V_{DD}		 0.1*V_{DD}	 V V
Load	I_{OUT}		15		pF
Output Rise /Fall Time[2] ≤20MHz 20.001 -50.000MHz 50.001-100.000MHz	t_R/t_F			 8 5 3	ns
Output Leakage, Output Disabled	I_Z			±10	uA
Duty Cycle[2,4]		45	50	55	%
Period Jitter[5], 100MHz RMS Peak-Peak	ϕJ		 2.4 23		ps
RMS Jitter[6,] 12k-20MHz	ϕJ		65	100	fs
Enable/Disable					
Output Enable/Disable[7] Output Enable Output Disable	 V_{IH} V_{IL}	 0.7*V_{DD}		 0.4	 V V
Disable time	t_D			100	ns
Start-Up Time	t_{SU}			10	ms
Operating Temp, (Ordering Option)	T_{OP}	-10/70, -40/85, -40/105, -40/125,-55/125			°C

1] The power supply should have by-pass capacitors as close to the supply and to ground as possible, for example 0.1 and 0.01uF.
2] Parameters are tested with the test circuit shown in Figure 1. Add ((50-15)(pF)*VDD*Fout(MHz)*0.001) mA for the 50pF option.
3] Includes initial accuracy, operating temp, supply voltage, shock and vibration (not under operation) and 10 years aging for ±50 and ±100 ppm options.
4] Duty Cycle is measured as On Time/Period, see Fig 2.
5] Broadband Period Jitter measured using a LeCroy Waverunner 610Zi, 100K samples.
6] Measured using an Agilent E5052 or equivalent, at 100MHz and 25°C.
7] The Output is Enabled if the Enable/Disable is left open, a 10K pull-up to Vdd is recommended.

Table 2. Electrical Performance, 3.3V Option					
Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply					
Voltage[1]	V_{DD}	2.97	3.3	3.63	V
Max Supply Voltage Max Voltage E/D		-0.5 -0.5		7.0 V_{DD}+0.5	V V
Current[2,] ≤12.MHz 12.001-20MHz 20.001- 65MHz 65.001-133MHz 133.001-160MHz	I_{DD}			 3 4 12 21 27	mA
Current, Output Disabled				10	uA
Frequency					
Nominal Frequency	f_N	1.024		160.000	MHz
Stability[3], (Ordering Option)		±25, ±32, ±50, ±100			ppm
Outputs					
Output Logic Levels[2] Output Logic High Output Logic Low	 V_{OH} V_{OL}	 0.9*V_{DD}		 0.1*V_{DD}	 V V
Load	I_{OUT}		15		pF
Output Rise /Fall Time[2] ≤20MHz 20.001 -50.000MHz 50.001-160.000MHz	t_R/t_F			 8 5 3	ns
Output Leakage, Output Disabled	I_Z			±10	uA
Duty Cycle[2,4]		45	50	55	%
Period Jitter[5], 100MHz RMS Peak-Peak	ϕJ		 2.8 25		ps
RMS Jitter[6,] 12k-20MHz	ϕJ		76	115	ps
Enable/Disable					
Output Enable/Disable[7] Output Enable Output Disable	 V_{IH} V_{IL}	 0.7*V_{DD}		 0.4	 V V
Disable time	t_D			100	ns
Start-Up Time	t_{SU}			10	ms
Operating Temp, (Ordering Option)	T_{OP}	-10/70, -40/85, -40/105, -40/125, -55/125			°C

1] The power supply should have by-pass capacitors as close to the supply and to ground as possible, for example 0.1 and 0.01uF.
2] Parameters are tested with the test circuit shown in Figure 1. Add ((50-15)(pF)*VDD*Fout(MHz)*0.001) mA for the 50pF option.
3] Includes initial accuracy, operating temp, supply voltage, shock and vibration (not under operation) and 10 years aging for ±50 and ±100 ppm options.
4] Duty Cycle is measured as On Time/Period, see Fig 2.
5] Broadband Period Jitter measured using a LeCroy Waverunner 610Zi, 100K samples.
6] Measured using an Agilent E5052 or equivalent, at 100MHz and 25°C.
7] The Output is Enabled if the Enable/Disable is left open, a 10K pull-up to Vdd is recommended.

Table 3. Electrical Performance, 2.5V Option					
Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply					
Voltage[1]	V_{DD}	2.25	2.5	2.75	V
Max Supply Voltage Max Voltage E/D		-0.5 -0.5		7.0 V_{DD}+0.5	V V
Current[2,] ≤12MHz 12.001-20MHz 20.001- 65MHz 65.001-133MHz 133.001-160MHz	I_{DD}			 2 3 9 16 23	mA
Current, Output Disabled				10	uA
Frequency					
Nominal Frequency	f_N	1.024		160.000	MHz
Stability[3,] (Ordering Option)		±25, ±32, ±50, ±100			ppm
Outputs					
Output Logic Levels[2] Output Logic High Output Logic Low	 V_{OH} V_{OL}	 0.9*V_{DD}		 0.1*V_{DD}	 V V
Load	I_{OUT}		15		pF
Output Rise /Fall Time[2] ≤20MHz 20.001 -50.000MHz 50.001-160.000MHz	t_R/t_F			 8 5 3	ns
Output Leakage, Output Disabled	I_Z			±10	uA
Duty Cycle[2,4]		45	50	55	%
Period Jitter[5], 100MHz RMS Peak-Peak	ϕJ		 2.8 26		ps
RMS Jitter[6,] 12k-20MHz	ϕJ		97	145	ps
Enable/Disable					
Output Enable/Disable[7] Output Enable Output Disable	 V_{IH} V_{IL}	 0.7*V_{DD}		 0.4	 V V
Disable time	t_D			100	ns
Start-Up Time	t_{SU}			10	ms
Operating Temp, (Ordering Option)	T_{OP}	-10/70, -40/85, -40/105, -40/125, -55/125			°C

1] The power supply should have by-pass capacitors as close to the supply and to ground as possible, for example 0.1 and 0.01uF.
2] Parameters are tested with the test circuit shown in Figure 1. Add ((50-15)(pF)*VDD*Fout(MHz)*0.001) mA for the 50pF option.
3] Includes initial accuracy, operating temp, supply voltage, shock and vibration (not under operation) and 10 years aging for ±50 and ±100 ppm options.
4] Duty Cycle is measured as On Time/Period, see Fig 2.
5] Broadband Period Jitter measured using a LeCroy Waverunner 610Zi, 100K samples.
6] Measured using an Agilent E5052 or equivalent, at 100MHz and 25°C.
7] The Output is Enabled if the Enable/Disable is left open, a 10K pull-up to Vdd is recommended.

Table 4. Electrical Performance, 1.8V Option					
Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply					
Voltage[1]	V_{DD}	1.71	1.8	1.89	V
Max Supply Voltage Max Voltage E/D		-0.5 -0.5		7.0 V_{DD}+0.5	V V
Current[2,] ≤12MHz 12.001-20MHz 20.001- 65MHz 65.001-133MHz 133.001-160MHz	I_{DD}			 2 3 7 13 19	mA
Current, Output Disabled				10	uA
Frequency					
Nominal Frequency	f_N	1.024		160.000	MHz
Stability[3], (Ordering Option)		±25, ±32, ±50, ±100			ppm
Outputs					
Output Logic Levels[2] Output Logic High Output Logic Low	 V_{OH} V_{OL}	 0.9*V_{DD}		 0.1*V_{DD}	 V V
Load	I_{OUT}		15		pF
Output Rise /Fall Time[2] ≤20MHz 20.001 -50.000MHz 50.001-160.000MHz	t_R/t_F			 8 5 3	ns
Output Leakage, Output Disabled	I_Z			±10	uA
Duty Cycle[2,4]		45	50	55	%
Period Jitter[5], 100MHz RMS Peak-Peak	ϕJ		 3.4 33		ps
RMS Jitter[6,] 12k-20MHz	ϕJ		212	320	ps
Enable/Disable					
Output Enable/Disable[7] Output Enable Output Disable	 V_{IH} V_{IL}	 0.7*V_{DD}		 0.4	 V V
Disable time	t_D			100	ns
Start-Up Time	t_{SU}			10	ms
Operating Temp, (Ordering Option)	T_{OP}	-10/70, -40/85, -40/105, -40/125, -55/125			°C

1] The power supply should have by-pass capacitors as close to the supply and to ground as possible, for example 0.1 and 0.01uF.
2] Parameters are tested with the test circuit shown in Figure 1. Add ((50-15)(pF)*VDD*Fout(MHz)*0.001) mA for the 50pF option.
3] Includes initial accuracy, operating temp, supply voltage, shock and vibration (not under operation) and 10 years aging for ±50 and ±100 ppm options.
4] Duty Cycle is measured as On Time/Period, see Fig 2.
5] Broadband Period Jitter measured using a LeCroy Waverunner 610Zi, 100K samples.
6] Measured using an Agilent E5052 or equivalent, at 100MHz and 25°C.
7] The Output is Enabled if the Enable/Disable is left open, a 10K pull-up to Vdd is recommended.

Test Diagram and Waveform

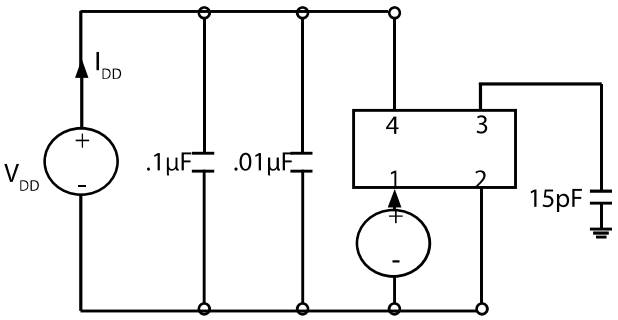


Fig 1: Test Circuit

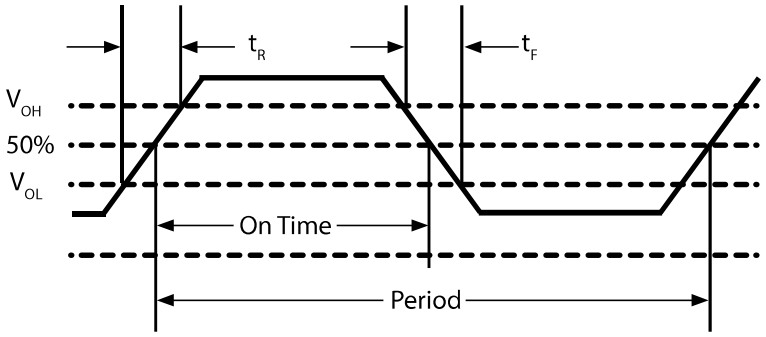
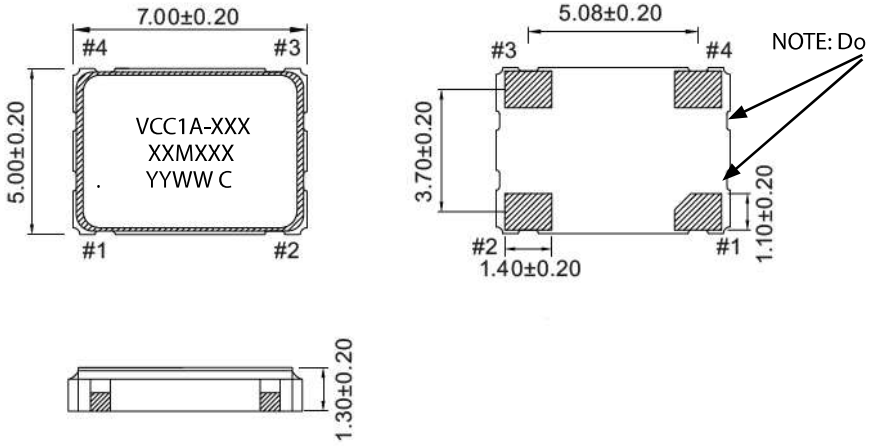
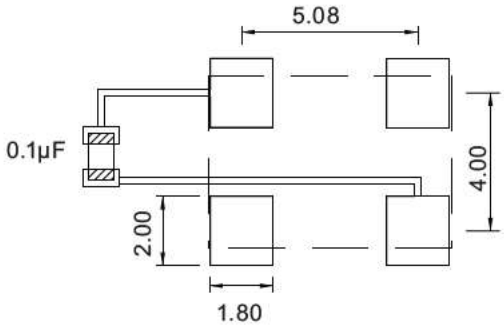


Fig 2: Waveform

Outline Drawing & Pad Layout



Dimensions in mm



Recommended Soldering Pad Layout

Marking
VCC1A = Product family, 7x5 ceramic XO
XXMXXX = Frequency, eg 50M000 = 50.000 MHz
. = Pin 1
YY = Year
WW = Week
C = Manufacturing location, eg C, J1, C3

Table 5. Pin Out

Pin	Symbol	Function
1	E/D	Enable Disable
2	GND	Case and Electrical Ground
3	Output	Output
4	V_{DD}	Power Supply Voltage

Table 6. Enable Disable Function

E/D Pin	Output
High	Clock Output
Open	Clock Output
Low	High Impedance

Reliability

Vectron qualification includes aging at various extreme temperatures, shock and vibration, temperature cycling, and IR reflow simulation. The VCC1A family is capable of meeting the following qualification tests:

Table 7. Environmental Compliance

Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Temperature Cycle	MIL-STD-883, Method 1010
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2015
Moisture Sensitivity Level	MSL 1
Contact Pads	Gold (0.3 um min to 1.0 um max) over Nickel
Contact Pads, _SNPB option	Tinned using solder alloy Sn63Pb37 in accordance with J-STD-006
Weight	178 mg

Although ESD protection circuitry has been designed into the VCC1A proper precautions should be taken when handling and mounting. Vectron employs a human body model (HBM) and a charged device model (CDM) for ESD susceptibility testing and design protection evaluation.

Table 8. ESD Ratings

Model	Minimum	Conditions
Human Body Model	400V	JES22-A115
Charged Device Model	2000V	JESD22-C101

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this datasheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability. Permanent damage is also possible if E/D is applied before V_{DD}.

Table 9. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Storage Temperature	TS	-55 to 125	°C
Soldering Temp/Time	T_{LS}	260 / 30	°C / sec

IR Reflow

The VCC1A is qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The VCC1A device is hermetically sealed so an aqueous wash is not an issue.

NOTE: Devices which have been solder dipped, _SNPB option, will not be Pb-Free.

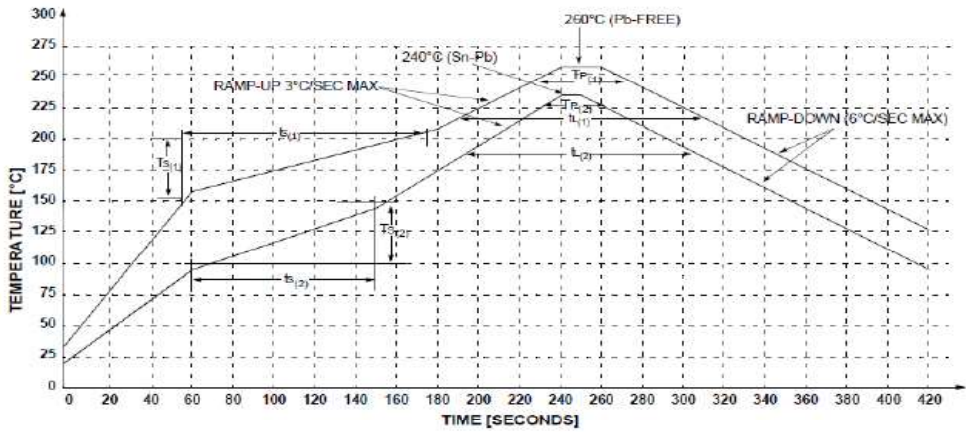


Table 10. Reflow Profile

Symbol	Min.	Max.	Units	Conditions
$Ts_{(1)}$	150	200	°C	Pb-Free
$Ts_{(2)}$	100	150	°C	_SNPB Option
$ts_{(1)}$	60	240	Sec	Pb-Free
$ts_{(2)}$	60	120	Sec	_SNPB Option
$tl_{(1)}$	60	150	Sec	Pb-Free
$tl_{(2)}$	60	150	Sec	_SNPB option
$Tp_{(1)}$	245	260	°C	Pb-Free
$Tp_{(2)}$	225	240	°C	_SNPB Option

Tape and Reel

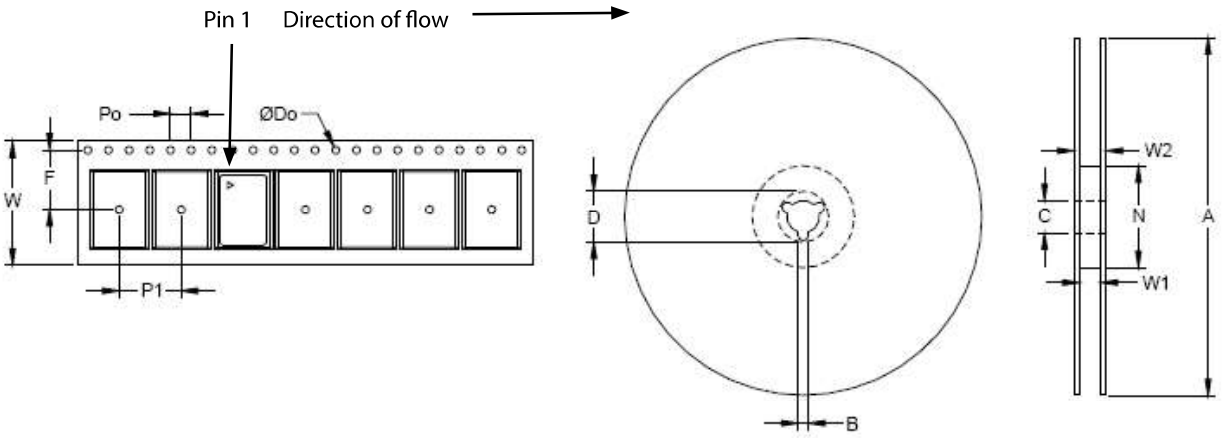


Table 11. Tape and Reel Information

Tape Dimensions (mm)						Reel Dimensions (mm)							
Dimension	W	F	Do	Po	P1	A	B	C	D	N	W1	W2	# Per Reel
Tolerance	Typ	Typ	Typ	Typ	Typ	Typ	Min	Typ	Min	Min	Typ	Max	
VCC1A	16	7.5	1.5	4	8	180	2	13	21	60	17	21	1000

Ordering Information

VCC1A- A3B- xxMxxxxxxxXX

Product
7x5 Crystal Oscillator

Power Supply
A: +5.0 Vdc, 15pF
B: +3.3 Vdc, 15pF
C: +3.0 Vdc, 15pF
E: +5.0 Vdc, 50pF
F: +3.3 Vdc, 50pF
G: +2.5 Vdc, 15pF
H: +1.8 Vdc, 15pF

Electrical Options:
3: Tri-state 45/55% Duty Cycle
The following codes are not recommended for new designs
0: No Tri-state, 40/60% Duty
1: Tri-state, 40/60% Duty
2: No tri-state, 45/55% Duty
5: Enable, 40/60% Duty
6: Enable, 45/55% Duty

Stability
A: ±100ppm over -10/70°C
B: ±50ppm over -10/70°C
C: ±100ppm over -40/85°C
D: ±50ppm over -40/85°C
E: ±25ppm over -10/70°C
F: ±25ppm over -40/85°C
K: ±32ppm over -10/70°C
O: ±32ppm over -40/85°C
S: ±100ppm over -40/105°C
V: ±100ppm over -40/125°C
P: ±100ppm over -55/125°C
R: ±50ppm over -55/125°C

Frequency in MHz

Packaging
TR: Tape and Reel
blank: Cut Tape / non Tape and Reel quantities
_SNPB: Tin Lead solder dipped

**Note: not all combination of options are available. Other specifications may be available upon request.*
50 pF load option is available at 3.3V and 5.0V, < 60MHz

Example:

VCC1A-A3D-100M000000TR	**Tape and Reel**
VCC1A-A3D-100M000000	**Cut Tape**
VCC1A-A3D-100M000000_SNPB	**Tin Lead solder dipped**

20ppm Stability Ordering Information

VCC1A-105-frequency = ±20ppm over -10/70°C, +5.0Vdc, 45/55% Duty Cycle, 15pF load
VCC1A-103-frequency = ±20ppm over -10/70°C, +3.3Vdc, 45/55% Duty Cycle, 15pF load
VCC1A-118-frequency = ±20ppm over -10/70°C, +2.5Vdc, 45/55% Duty Cycle, 15pF load
VCC1A-119-frequency = ±20ppm over -10/70°C, +1.8Vdc, 45/55% Duty Cycle, 15pF load

Example:

VCC1A-105-19M4400000TR	**Tape and Reel**
VCC1A-105-19M4400000	**Cut Tape**
VCC1A-105-19M4400000_SNPB	**Tin lead solder dipped**

Revision History

Revision Date	Approved	Description
August15, 2022		

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