


Helping Customers Innovate, Improve & Grow



Description

Vectron's VCC1A Crystal Oscillator (XO) is a quartz stabilized square wave generator with a CMOS output. The VCC1A uses a fundamental or 3rd overtone crystal resulting in very low jitter performance, and a monolithic IC which improves reliability and reduces cost.

Features

- Ultra Low Jitter, Fundamental or 3rd OT Crystal Design
- CMOS Output Crystal Oscillator
- Output Frequencies from 1.024 MHz to 160.000 MHz
- +1.8, +2.5, +3.3 or +5.0V Operation
- Output Disable Feature
- Excellent ± 25 ppm temperature stability
- -10/70°C, -40/85°C or -40/105°C operating temperature
- Small Industry Standard Package, 7 x 5 mm
- Product is compliant to RoHS directive  and fully compatible with lead free assembly

Applications

- SONET/SDH/DWDM
- Ethernet, GE, SynchE
- Storage Area Networking
- Fiber Channel
- Digital Video
- Broadband Access
- Base Stations, Picocells
- Driving A/D's, D/A's, FPGA's
- Test and Measurement
- COTS

Block Diagram

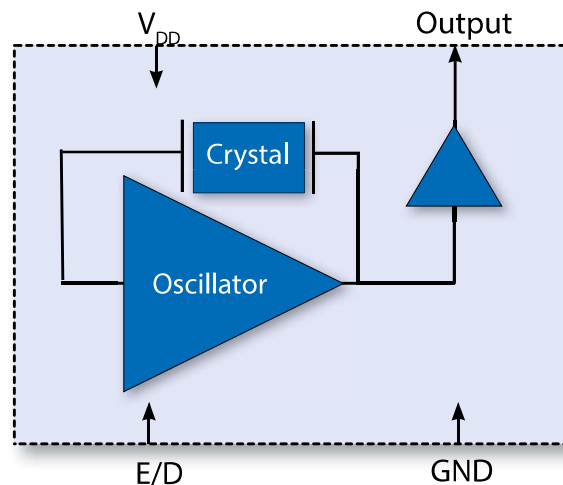


Table 1. Electrical Performance, 5V

Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply					
Voltage ¹	V_{DD}	4.5	5.0	5.5	V
Max Supply Voltage		-0.5		7.0	V
Max Voltage E/D		-0.5		$V_{DD}+0.5$	V
Current ² ≤20MHz 20.001-65.000MHz 65.001-100MHz	I_{DD}			10 30 40	mA
Current, Output Disabled				10	uA
Frequency					
Nominal Frequency ³	f_N	1.024		100.000	MHz
Stability ⁴ , (Ordering Option)		±25, ±32, ±50, ±100			ppm
Outputs					
Output Logic Levels ² Output Logic High Output Logic Low	V_{OH} V_{OL}	$0.9*V_{DD}$		$0.1*V_{DD}$	V V
Load	I_{OUT}		15	30	pF
Output Rise /Fall Time ² ≤20MHz 20.001 -50.000MHz 50.001-100.000MHz	t_R/t_F			8 5 3	ns
Output Leakage, Output Disabled	I_Z			±10	uA
Duty Cycle ^{2,5}		45	50	55	%
Period Jitter ⁶ , 100MHz RMS Peak-Peak	ϕ_J				ps
RMS Jitter ⁷ , 12k-20MHz	ϕ_J				ps
Enable/Disable					
Output Enable/Disable ⁸ Output Enable Output Disable	V_{IH} V_{IL}	$0.7*V_{DD}$		0.4	V V
Disable time	t_D			100	ns
Start-Up Time	t_{SU}			10	ms
Operating Temp, (Ordering Option)	T_{OP}	-10/70, -40/85, -40/105			°C

1] The power supply should have by-pass capacitors as close to the supply and to ground as possible, for example 0.1 and 0.01 uF.

2] Parameters are tested with the test circuit shown in Figure 1.

3] See Standard Frequencies and Ordering Information tables for more specific information.

4] Includes initial accuracy, operating temperature, supply voltage, shock and vibration (not under operation) and 10 years aging.

5] Duty Cycle is measured as On Time/Period, see Fig 2.

6] Broadband Period Jitter measured using a LeCroy Wavemaster 8600A, 90K samples, see Application Note for Typical Phase Noise and Jitter Performance.

7] Measured using an Agilent E5052 or equivalent, at 50MHz

8] The Output is Enabled if the Enable/Disable is left open.

Table 2. Electrical Performance, 3.3V

Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply					
Voltage ¹	V_{DD}	2.97	3.3	3.63	V
Max Supply Voltage		-0.5		7.0	V
Max Voltage E/D		-0.5		$V_{DD}+0.5$	V
Current ² ≤20MHz 20.001-65.000MHz 65.001-160MHz	I_{DD}			10 30 40	mA
Current, Output Disabled				10	uA
Frequency					
Nominal Frequency ³	f_N	1.024		160.000	MHz
Stability ⁴ , (Ordering Option)		±25, ±32, ±50, ±100			ppm
Outputs					
Output Logic Levels ² Output Logic High Output Logic Low	V_{OH} V_{OL}	0.9* V_{DD}		0.1* V_{DD}	V V
Load	I_{OUT}		15	30	pF
Output Rise /Fall Time ² ≤20MHz 20.001 -50.000MHz 50.001-160.000MHz	t_R/t_F			8 5 3	ns
Output Leakage, Output Disabled	I_Z			±10	uA
Duty Cycle ^{2,5}		45	50	55	%
Period Jitter ⁶ , 100MHz RMS Peak-Peak	ϕ_J				ps
RMS Jitter ⁷ , 12k-20MHz	ϕ_J				ps
Enable/Disable					
Output Enable/Disable ⁸ Output Enable Output Disable	V_{IH} V_{IL}	0.7* V_{DD}		0.4	V V
Disable time	t_D			100	ns
Start-Up Time	t_{SU}			10	ms
Operating Temp, (Ordering Option)	T_{OP}	-10/70, -40/85, -40/105			°C

1] The power supply should have by-pass capacitors as close to the supply and to ground as possible, for example 0.1 and 0.01 uF.

2] Parameters are tested with the test circuit shown in Figure 1.

3] See Standard Frequencies and Ordering Information tables for more specific information.

4] Includes initial accuracy, operating temperature, supply voltage, shock and vibration (not under operation) and 10 years aging.

5] Duty Cycle is measured as On Time/Period, see Fig 2.

6] Broadband Period Jitter measured using a LeCroy Wavemaster 8600A, 90K samples, see Application Note for Typical Phase Noise and Jitter Performance.

7] Measured using an Agilent E5052 or equivalent, at 50MHz

8] The Output is Enabled if the Enable/Disable is left open.

Table 3. Electrical Performance, 2.5V

Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply					
Voltage ¹	V_{DD}	2.25	2.5	2.75	V
Max Supply Voltage		-0.5		7.0	V
Max Voltage E/D		-0.5		$V_{DD}+0.5$	V
Current ² ≤20MHz 20.001-65.000MHz 65.001-160MHz	I_{DD}			10 30 40	mA
Current, Output Disabled				10	uA
Frequency					
Nominal Frequency ³	f_N	1.024		160.000	MHz
Stability ⁴ , (Ordering Option)		±25, ±32, ±50, ±100			ppm
Outputs					
Output Logic Levels ² Output Logic High Output Logic Low	V_{OH} V_{OL}	$0.9*V_{DD}$		$0.1*V_{DD}$	V V
Load	I_{OUT}		15	30	pF
Output Rise /Fall Time ² ≤20MHz 20.001 -50.000MHz 50.001-160.000MHz	t_R/t_F			8 5 3	ns
Output Leakage, Output Disabled	I_Z			±10	uA
Duty Cycle ^{2,5}		45	50	55	%
Period Jitter ⁶ , 100MHz RMS Peak-Peak	ϕ_J				ps
RMS Jitter ⁷ , 12k-20MHz	ϕ_J				ps
Enable/Disable					
Output Enable/Disable ⁸ Output Enable Output Disable	V_{IH} V_{IL}	$0.7*V_{DD}$		0.4	V V
Disable time	t_D			100	ns
Start-Up Time	t_{SU}			10	ms
Operating Temp, (Ordering Option)	T_{OP}	-10/70, -40/85, -40/105			°C

1] The power supply should have by-pass capacitors as close to the supply and to ground as possible, for example 0.1 and 0.01 uF.

2] Parameters are tested with the test circuit shown in Figure 1.

3] See Standard Frequencies and Ordering Information tables for more specific information.

4] Includes initial accuracy, operating temperature, supply voltage, shock and vibration (not under operation) and 10 years aging.

5] Duty Cycle is measured as On Time/Period, see Fig 2.

6] Broadband Period Jitter measured using a LeCroy Wavemaster 8600A, 90K samples, see Application Note for Typical Phase Noise and Jitter Performance.

7] Measured using an Agilent E5052 or equivalent, at 50MHz

8] The Output is Enabled if the Enable/Disable is left open.

Table 4. Electrical Performance, 1.8V

Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply					
Voltage ¹	V_{DD}	1.71	1.8	1.89	V
Max Supply Voltage		-0.5		7.0	V
Max Voltage E/D		-0.5		$V_{DD}+0.5$	V
Current ² ≤20MHz 20.001-65.000MHz 65.001-160MHz	I_{DD}			10 30 40	mA
Current, Output Disabled				10	uA
Frequency					
Nominal Frequency ³	f_N	1.024		160.000	MHz
Stability ⁴ , (Ordering Option)		±25, ±32, ±50, ±100			ppm
Outputs					
Output Logic Levels ² Output Logic High Output Logic Low	V_{OH} V_{OL}	$0.9*V_{DD}$		$0.1*V_{DD}$	V V
Load	I_{OUT}		15	30	pF
Output Rise /Fall Time ² ≤20MHz 20.001 -50.000MHz 50.001-160.000MHz	t_R/t_F			8 5 3	ns
Output Leakage, Output Disabled	I_Z			±10	uA
Duty Cycle ^{2,5}		45	50	55	%
Period Jitter ⁶ , 100MHz RMS Peak-Peak	ϕ_J				ps
RMS Jitter ⁷ , 12k-20MHz	ϕ_J				ps
Enable/Disable					
Output Enable/Disable ⁸ Output Enable Output Disable	V_{IH} V_{IL}	$0.7*V_{DD}$		0.4	V V
Disable time	t_D			100	ns
Start-Up Time	t_{SU}			10	ms
Operating Temp, (Ordering Option)	T_{OP}	-10/70, -40/85, -40/105			°C

1] The power supply should have by-pass capacitors as close to the supply and to ground as possible, for example 0.1 and 0.01uF.

2] Parameters are tested with the test circuit shown in Figure 1.

3] See Standard Frequencies and Ordering Information tables for more specific information.

4] Includes initial accuracy, operating temperature, supply voltage, shock and vibration (not under operation) and 10 years aging.

5] Duty Cycle is measured as On Time/Period, see Fig 2.

6] Broadband Period Jitter measured using a LeCroy Wavemaster 8600A, 90K samples, see Application Note for Typical Phase Noise and Jitter Performance.

7] Measured using an Agilent E5052 or equivalent, at 50MHz

8] The Output is Enabled if the Enable/Disable is left open.

Test Diagram and Waveform

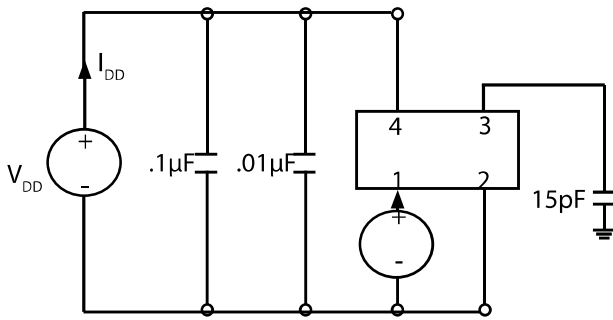


Fig 1: Test Circuit

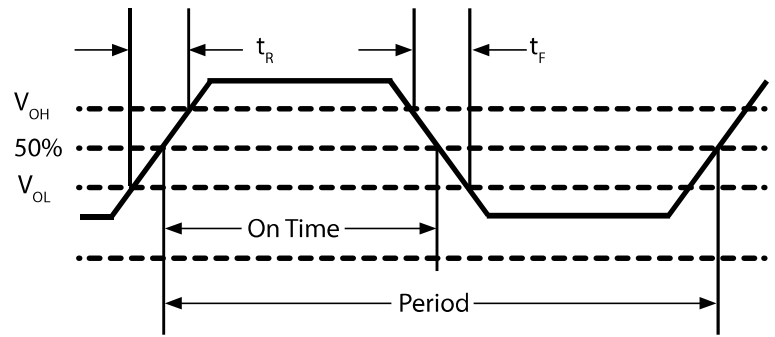


Fig 2: Waveform

Outline Drawing & Pad Layout

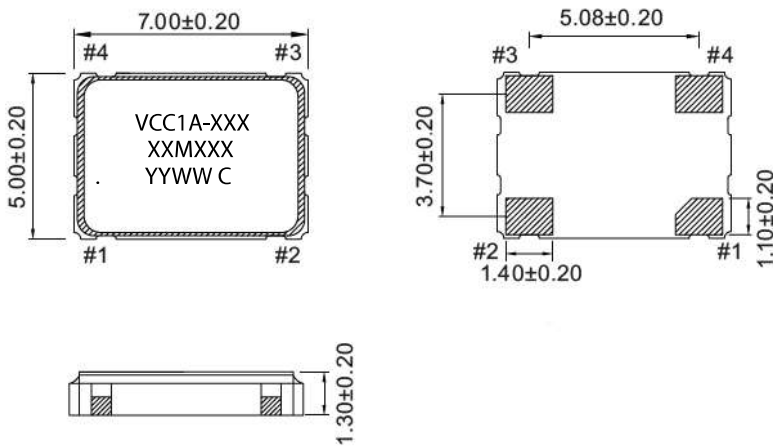


Table 5. Pin Out

Pin	Symbol	Function
1	E/D	Enable Disable
2	GND	Case and Electrical Ground
3	Output	Output
4	V_{DD}	Power Supply Voltage

Table 6. Enable Disable Function

E/D Pin	Output
High	Clock Output
Open	Clock Output
Low	High Impedance

Dimensions in mm

Marking

VCC1A = Product family, 7x5 ceramic XO
 XXMXXX = Frequency, eg 50M000 = 50.000 MHz
 . = Pin 1
 YY = Year
 WW = Week
 C = Manufacturing location

Recommended Soldering Pad Layout

Reliability

Vectron qualification includes aging at various extreme temperatures, shock and vibration, temperature cycling, and IR reflow simulation. The VCC1A family is capable of meeting the following qualification tests:

Table 7. Environmental Compliance	
Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Temperature Cycle	MIL-STD-883, Method 1010
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2015
Moisture Sensitivity Level	MSL 1
Contact Pads	Gold (0.3 um min to 1.0 um max) over Nickel
Weight	178 mg

Although ESD protection circuitry has been designed into the VCC1A proper precautions should be taken when handling and mounting. Vectron employs a human body model (HBM) and a charged device model (CDM) for ESD susceptibility testing and design protection evaluation.

Table 8. ESD Ratings		
Model	Minimum	Conditions
Human Body Model	400V	JES22-A115
Charged Device Model	2000V	JESD22-C101

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this datasheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability. Permanent damage is also possible if E/D is applied before V_{DD} .

Table 9. Absolute Maximum Ratings			
Parameter	Symbol	Ratings	Unit
Storage Temperature	T_S	-55 to 125	°C
Soldering Temp/Time	T_{LS}	260 / 30	°C / sec

IR Reflow

The VCC1A is qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The VCC1A device is hermetically sealed so an aqueous wash is not an issue.

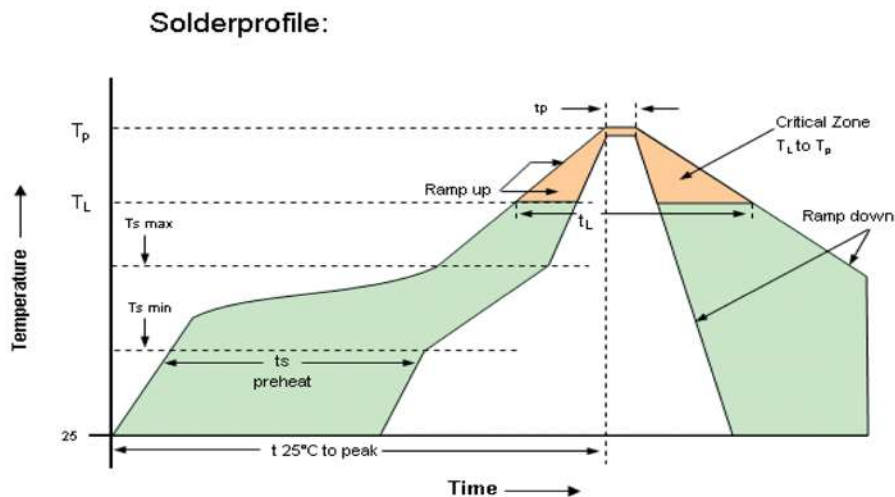


Table 10. Reflow Profile

Parameter	Symbol	Value
PreHeat Time Ts-min Ts-max	t_s	60 sec Min, 260 sec Max 150°C 200°C
Ramp Up	R_{UP}	3 °C/sec Max
Time Above 217 °C	t_L	60 sec Min, 150 sec Max
Time To Peak Temperature	T_{AMB-P}	480 sec Max
Time at 260 °C	t_p	30 sec Max
Ramp Down	R_{DN}	6 °C/sec Max

Tape and Reel

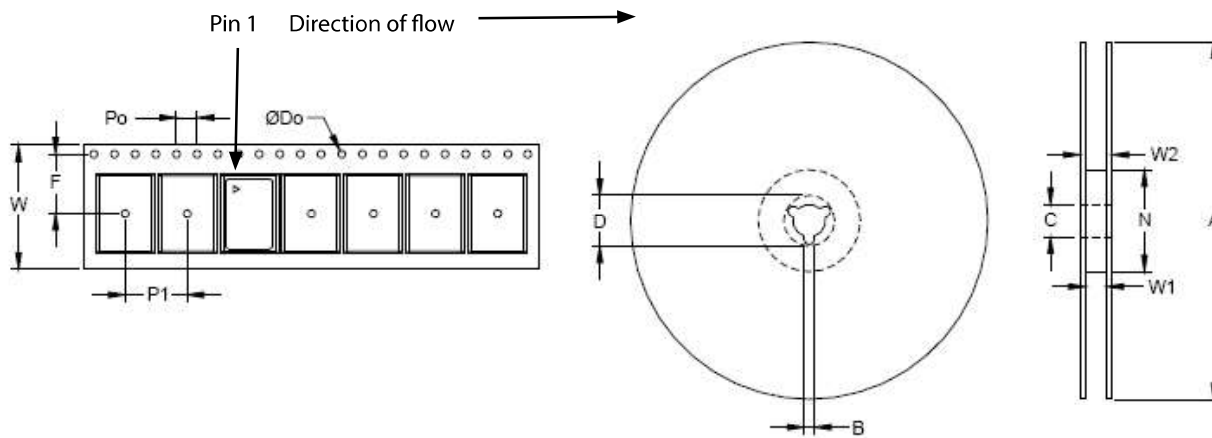


Table 11. Tape and Reel Information

Tape Dimensions (mm)						Reel Dimensions (mm)							
Dimension	W	F	Do	Po	P1	A	B	C	D	N	W1	W2	# Per Reel
Tolerance	Typ	Typ	Typ	Typ	Typ	Typ	Min	Typ	Min	Min	Typ	Max	
VCC1A	16	7.5	1.5	4	8	180	2	13	21	60	17	21	1000

Ordering Information

VCC1A- A3B- xxMxxxxxxxxXX

Product

7x5 Crystal Oscillator

Power Supply

- A: +5.0 Vdc
- B: +3.3 Vdc
- G: +2.5 Vdc
- H: +1.8 Vdc

Electrical Options:
3: Tri-state 45/55% Duty Cycle

Packaging

- TR: Tape and Reel
- blank: Cut Tape / non Tape and Reel quantities

Frequency in MHz

Stability

- A: ±100ppm over -10/70°C
- B: ±50ppm over -10/70°C
- C: ±100ppm over -40/85°C
- D: ±50ppm over -40/85°C
- E: ±25ppm over -10/70°C
- F: ±25ppm over -40/85°C
- K: ±32ppm over -10/70°C
- O: ±32ppm over -40/85°C
- S: ±100ppm over -40/105°C

*Note: not all combination of options are available.
 Other specifications may be available upon request.

Example:

VCC1A-A3D-100M000000TR
 VCC1A-A3D-100M000000

Tape and Reel
Cut Tape

Revision History

Revision Date	Approved	Description
Feb 23, 2022		

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