

Helping Customers Innovate, Improve & Grow



Description

The VS-800 is a Voltage Controlled SAW Oscillator that operates at the fundamental frequency of the internal SAW resonator. The SAW resonator is a high-Q Quartz device that enables the circuit to achieve ultra-low phase jitter performance over a wide operating temperature range. An internal multiplier circuit is deployed for output frequencies above 1.6 GHz. The oscillator is housed in a hermetically sealed leadless surface mount package and offered on tape and reel. It has an Output Enable function that provides the conditions: Outputs Enabled, or Outputs Disabled.

Features

- Industry Standard Package: 5.0 x 3.2 x 1.8 mm³
- Output Frequencies: 800 MHz to 3.2 GHz
- Next Generation ASIC Technology for Ultra-Low Jitter
 - 60 fs-rms ($f_N = 1.56897$ GHz, 1 kHz to 40 MHz)
 - 6 fs-rms ($f_N = 1.56897$ GHz, 12 kHz to 20 MHz)
 - 10 fs-rms ($f_N = 1.56897$ GHz, 10 kHz to 100 MHz)
- Absolute Pull Range: ± 20 ppm
- Supply Voltage: 3.3 V
- Differential or Single Ended Sinewave Output
- Output Enable / Disable (OE / OD)
- Compliant to EU RoHS6 Directive 

Applications

- High Speed Data Converters (ADC / DAC)
- Optical Transport Networks (40G / 100G / 200G / 400G)
- Wireless Communication
- Cable Modem Termination Systems (DOCSIS)
- High-Rel. Applications

Block Diagram

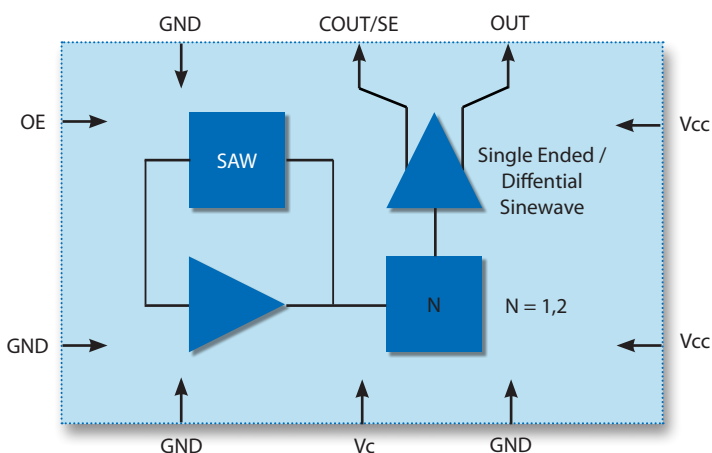


Figure 1. Functional block diagram

Performance Specifications

Electrical Performance						
Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Frequency						
Fundamental Frequency	f_N		800-1600		MHz	
2x Frequency Multiplier	f_N		1600-3200		MHz	
Temperature Stability (-40°C to +85°C)	f_{TEMP}		±100		ppm	
Supply Voltage Sensitivity		-10		+10	ppm	1
Load pull			1	10	ppm	3
Absolute Pull Range	APR		±20		ppm	
Supply						
Voltage (± 5%)	V_{CC}	3.14	3.3	3.46	V	
Current (Typical 50 Ω Load)	I_{CC}		75	150	mA	6
Control Voltage Input						
Control Voltage Range	V_C	0		V_{CC}	V	
Gain Transfer	K_V		+110		ppm/V	2
Total Pull	T_{PULL}		300		ppm	2
Linearity	L_{VC}		±7		%	2
Gain Transfer Ratio	$K_{V_{MAX}} / K_{V_{MIN}}$		< 2.75:1			2
Modulation Bandwidth	BW		100		kHz	
RF Output (Sinewave)						
Output Power (Single Ended, 1x)	CLK	3	5	8	dBm	3
Output Power (Differential, 1x)	CLK±	-3	0	3	dBm	3,7
Output Power (Single Ended, 2x)	CLK	TBD	TBD	TBD	dBm	3
Output Power (Differential, 2x)	CLK±	-3	0	3	dBm	3,7
Sub-Harmonics Suppression (2x Multiplier)			>25		dBc	
Phase Noise @ 10 Hz			-33		dBc/Hz	4
Phase Noise @ 100 Hz			-65		dBc/Hz	4
Phase Noise @ 1 kHz			-95		dBc/Hz	4
Phase Noise @ 10 kHz			-125		dBc/Hz	4
Phase Noise @ 100 kHz			-145		dBc/Hz	4
Phase Noise @ 1 MHz			-164		dBc/Hz	4
Phase Noise @ 10 MHz			-172		dBc/Hz	4
Phase Noise @ 100 MHz			-164		dBc/Hz	4
Jitter (1 kHz - 40 MHz)	Φ_J		60		fs-rms	4,5
Jitter (12 kHz - 20 MHz)	Φ_J		6		fs-rms	4,5
Jitter (10 kHz - 100 MHz)	Φ_J		10		fs-rms	4,5
Operating Temperature	T_{OP}	-40		+85	°C	
Package Size		5.0 x 3.2 x 1.8			mm ³	

Notes:

1. V_{CC} : 3.3 V ± 5%
2. V_C : 0 V to V_{CC}
3. Load Impedance 50 Ohm with VSWR ≤ 1.5:1
4. For carrier frequency 1.56897 GHz, DIFF1X output configuration
5. Place 1 µF, 10 nF bypass capacitors close to V_{CC} pads
6. Maximum current consumption is depending on output configuration
7. Output power measured single ended with other output terminated to 50 Ohm

Absolute Maximum Ratings

Absolute Maximum Ratings			
Parameter	Symbol	Ratings	Unit
Power Supply	V_{CC}	4	V
Input Current	I_{IN}	150	mA
Output Current	I_{OUT}	25	mA
Voltage Control	V_C	V_{CC}	V
Output Enable	OE	V_{CC}	V
Storage Temperature	T_{STR}	-55 to +125	°C
Soldering Temperature / Duration	T_{PEAK} / t_P	260 / 40	°C/s

Stresses in excess of the absolute maximum ratings can permanently damage the device. Also, exposure to these absolute maximum ratings for extended periods may adversely affect device reliability. Functional operation is not implied at these or any other conditions in excess of those represented in the operational sections of this datasheet.

Typical Performance Characteristics: Vc Pull (DIFF 1x output configuration)

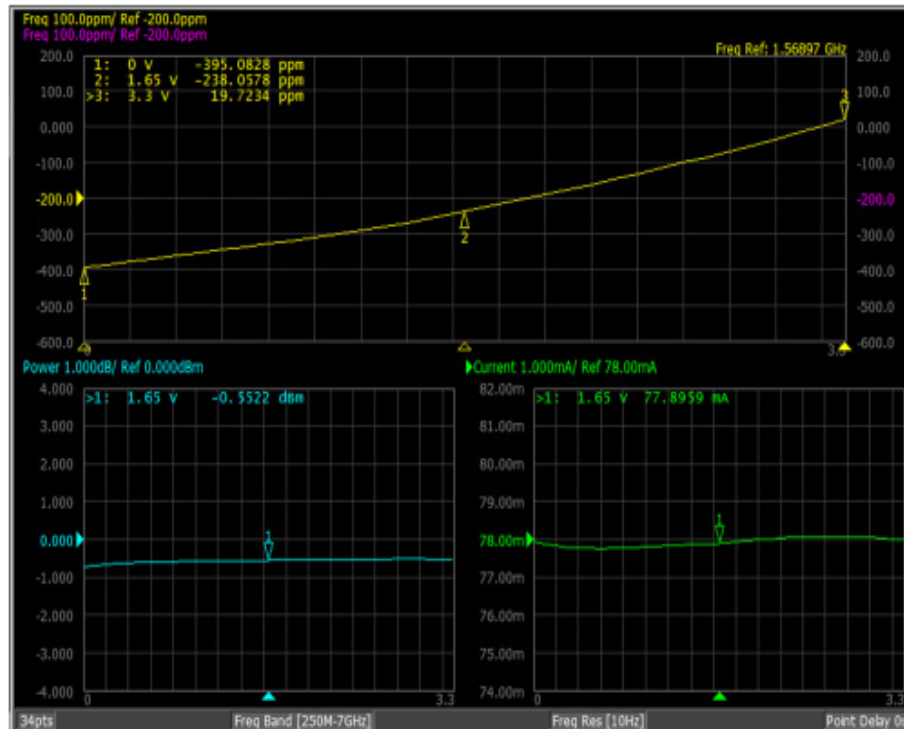


Figure 2. Vc Pull Performance Characteristics @ 1.56897 GHz

Typical Characteristics: Phase Noise @ 1.56897 GHz (DIFF 1X output configuration)

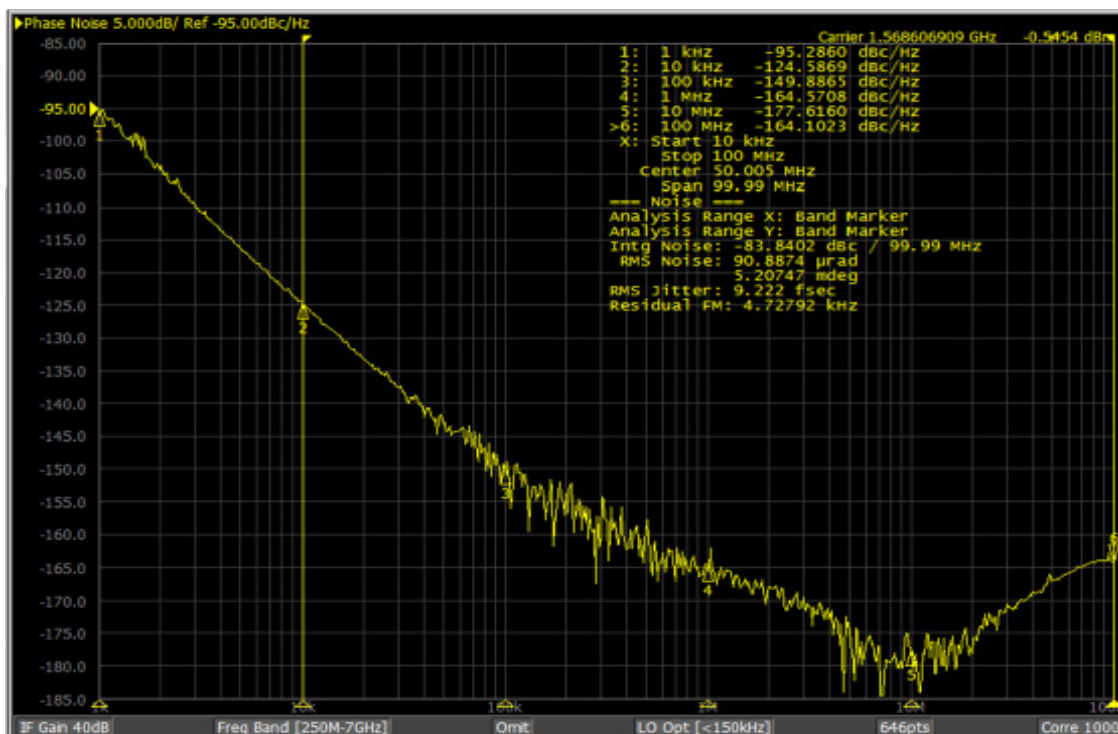


Figure 3. Typical Phase Noise Performance @ 1.56897 GHz

Typical Characteristics: Phase Noise @ 3.13794 GHz (DIFF 2X output configuration)

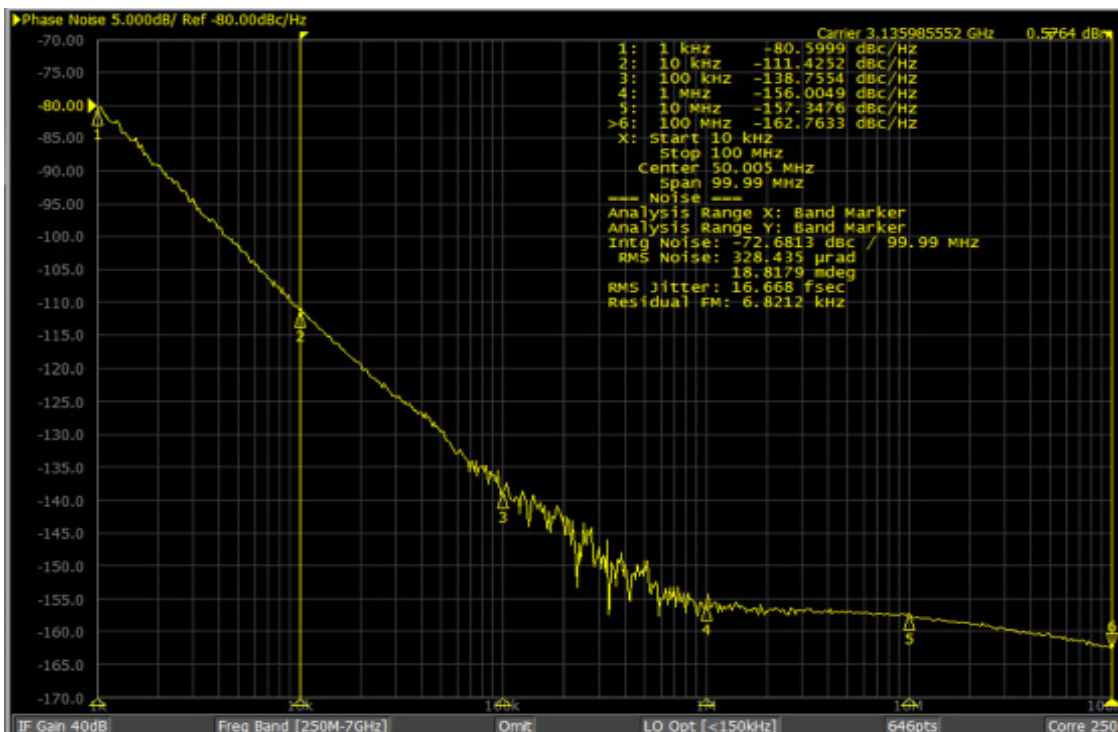


Figure 4. Typical Phase Noise Performance @ 3.13794 GHz

Typical Characteristics: Phase Noise @ 1.56897 GHz (SE 1X output configuration)

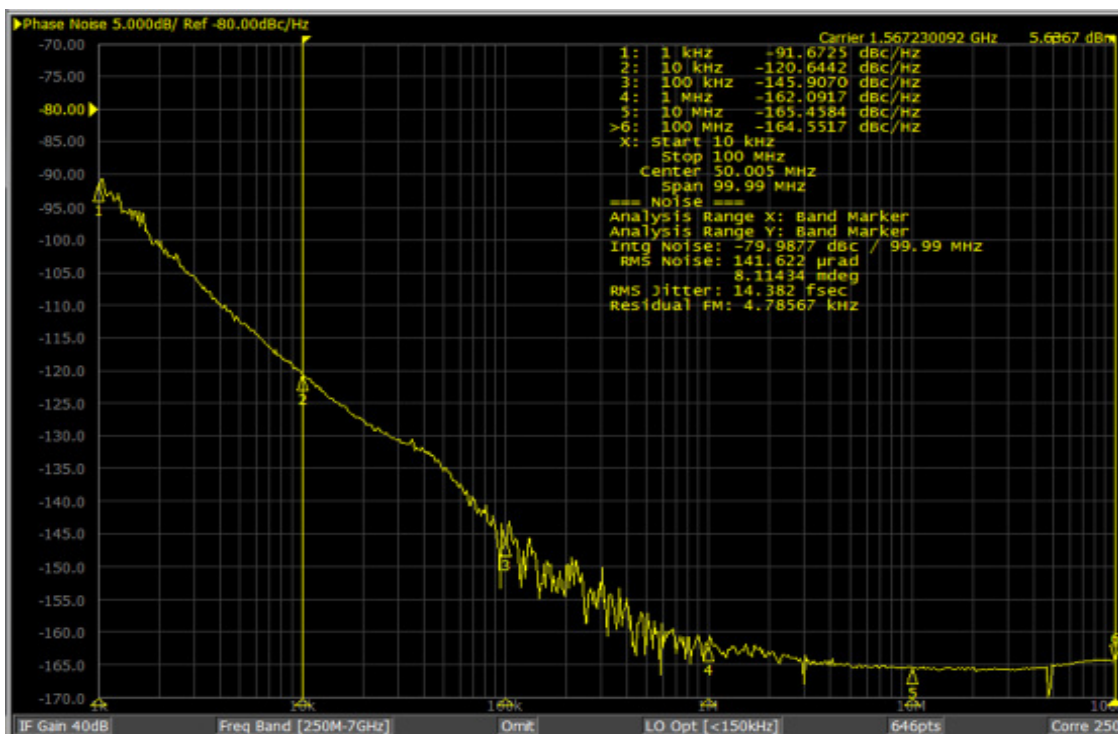


Figure 5. Typical Phase Noise Performance @ 1.56897 GHz

Typical Characteristics: Phase Noise @ 3.13794 GHz (SE 2X output configuration)

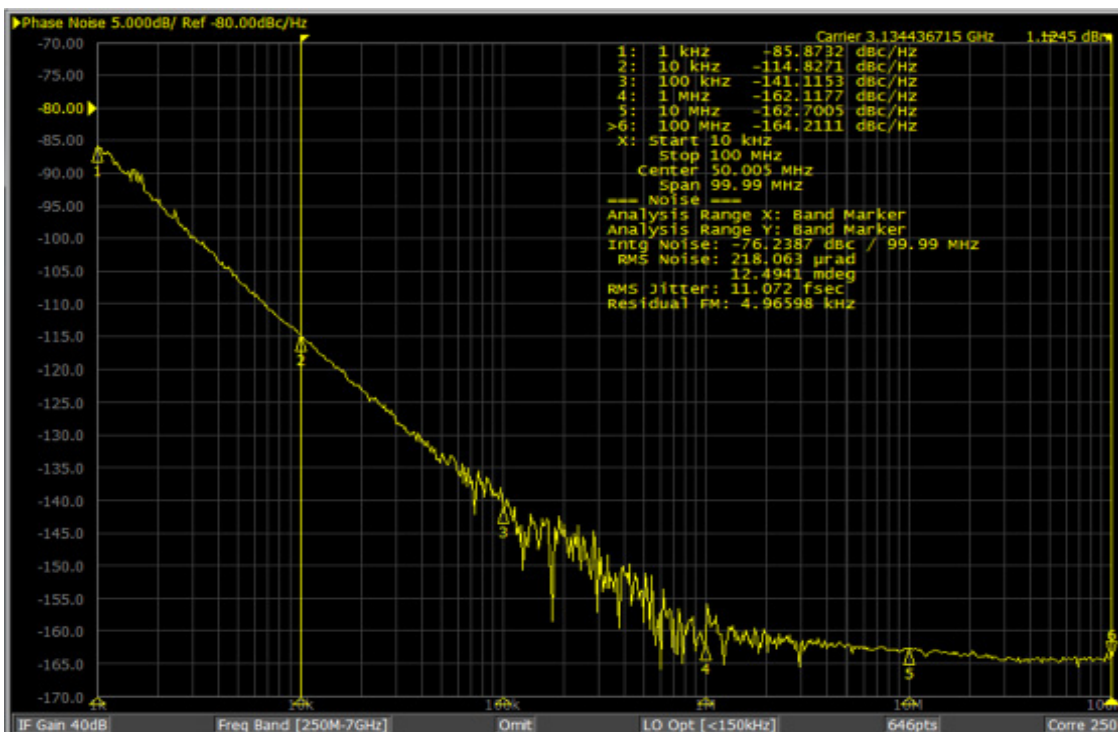


Figure 6. Typical Phase Noise Performance @ 3.13794 GHz

Reliability

VI qualification includes aging at various extreme temperatures, shock and vibration, temperature cycling, and IR reflow simulation. The VS-800 family is capable of meeting the following qualification tests:

Environmental Compliance	
Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2016
Moisture Sensitivity Level	IPC/JEDEC J-STD-020, MSL1

Handling Precautions

Although ESD protection circuitry has been designed into the VS-800 proper precautions should be taken when handling and mounting. VI employs a Human Body Model (HBM), a Charged Device Model (CDM), and a Machine Model (MM) for ESD susceptibility testing and design protection evaluation.

ESD Ratings		
Model	Minimum	Conditions
Human Body Model	2000 V	MIL-STD 883, Method 3015
Charged Device Model	1000 V	JEDEC, JESD22-C101
Machine Model	200 V	JEDEC, JESD22-A115-A

Reflow Profile (IPC/JEDEC J-STD-020)		
Parameter	Symbol	Value
PreHeat Time	t_s	60 s min., 180 s max.
Ramp Up	R_{UP}	3°C / s max.
Time Above 217°C	t_L	60 s min., 150 s max.
Time To Peak Temperature	t_{AMB-P}	480 s max.
Time At 260°C	t_P	20 s min., 40 s max.
Ramp Down	R_{DN}	6°C / s max.

The device has been qualified to meet the JEDEC standard for Pb-free assembly. The temperatures and time intervals listed are based on the Pb-free small body requirements. The temperatures refer to the topside of the package, measured on the package body surface. The VS-800 device is hermetically sealed so an aqueous wash is not an issue.

Terminal Plating: Electroless Au > 1.50 μm over
Electroless Ni > 1.90 μm

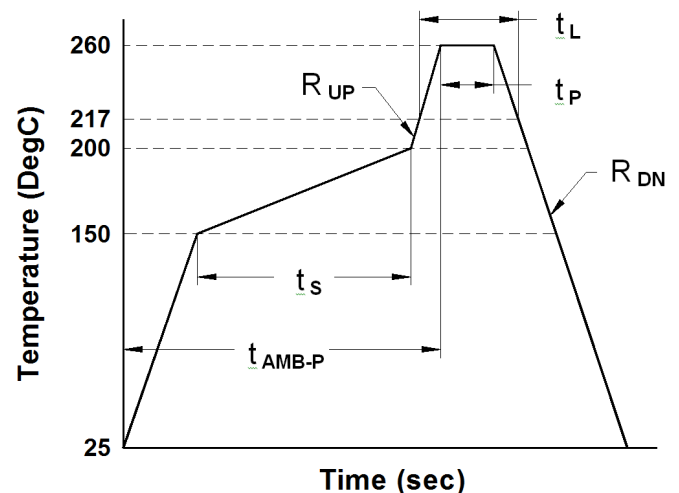
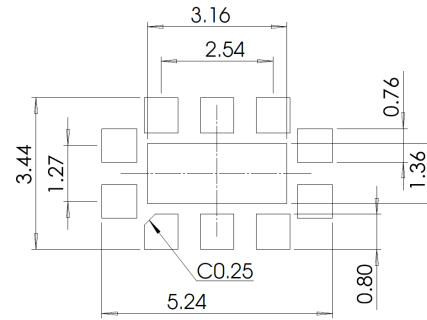
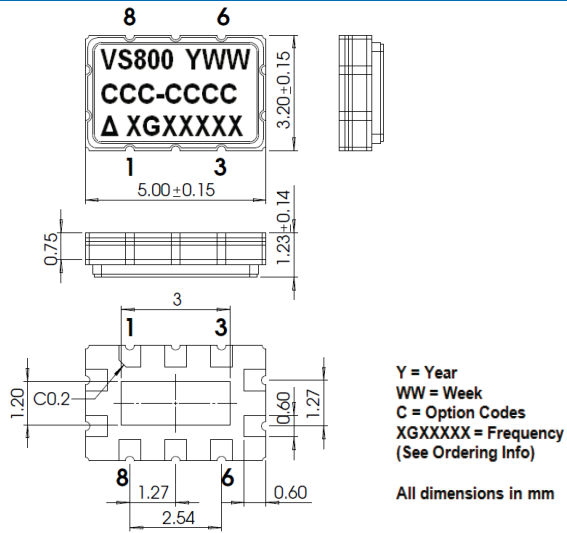


Figure 7. Recommended Reflow Profile

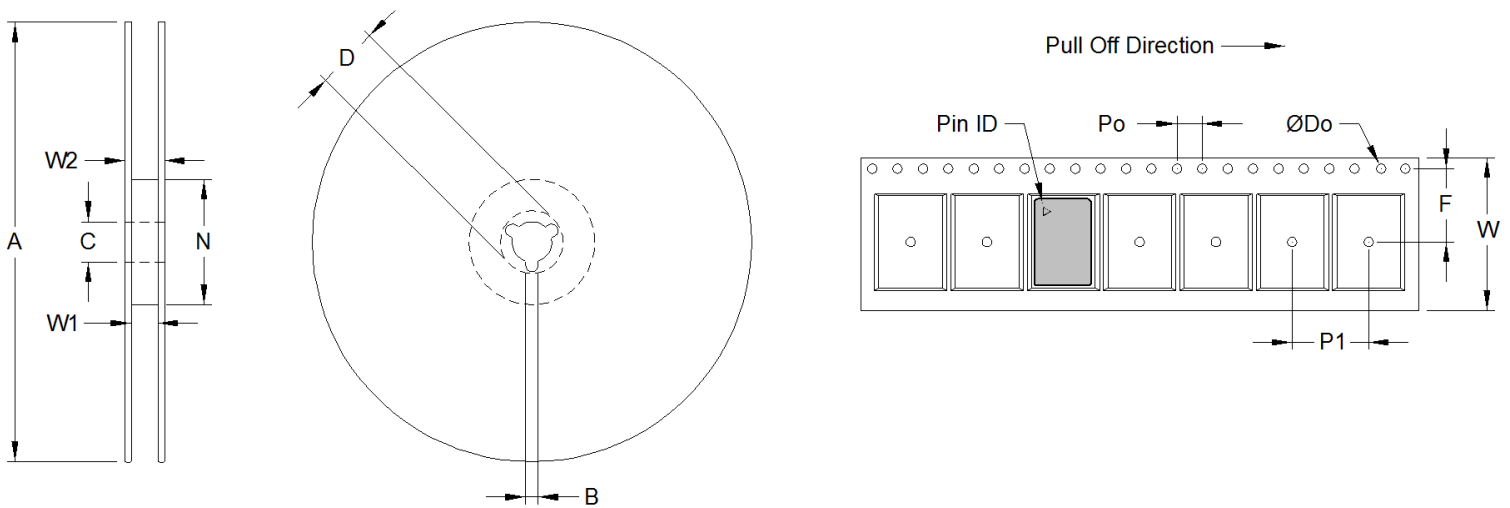
Outline Drawing & Pad Layout



Pin Out		
Pin	Symbol	Function
1	GND	Case and Electrical Ground
2	V _c	Control Voltage
3	GND	Case and Electrical Ground
4	V _{CC}	Supply Voltage
5	V _{CC}	Supply Voltage
6	OUT	Differential Output
7	COUT/SE	Complementary Differential Output / Single Ended Output
8	GND	Case and Electrical Ground
9	OE	Output Enable
10	GND	Case and Electrical Ground
Center	GND	Case and Electrical Ground

Output Enable		
Level	Voltage Range	Result
H	> V _{CC} -0.5 V	Output Enabled (OE)
L	< 0.5V	Output Disabled (OD)

Tape and Reel (EIA-481-2-A)



Tape Dimensions (mm)						Reel Dimensions (mm)							
Dimension	W	F	Do	Po	P1	A	B	C	D	N	W1	W2	#Per Reel
Tolerance	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Min.	Typ.	Min.	Min.	Typ.	Max.	
VS-800	16	7.5	1.5	4	8	178	1.5	13	20.2	50	16.4	22.4	200

Ordering Information

Standard Frequencies (MHz)						
800.000000	983.040000	993.409690				

Standard Frequencies (GHz)						
1.22880000	1.47456000	1.56897000	1.60000000	1.96608000	2.45760000	2.50000000
2.94912000						

Other Frequencies Available Upon Request

Ordering Information

VS- 800 - E G U - A A N N - xGxxxxxxxxx

Product Family

VS: VCSO

Package

800: 5.0 x 3.2 x 1.8 mm³

Supply Voltage

E: 3.3 V

Output

E: Single Ended Sinewave

G: Differential Sinewave

Operating Temperature

U: 0°C to 85°C

E: -40°C to 85°C

Absolute Pull Range

A: ± 5 ppm

E: ± 20 ppm

Frequency (See Above)

800M000000 - 3G20000000

Factory Use

N: N/A

Factory Use

N: N/A

Control Logic (Float Condition)

A: L=OD, H=OE, Float = OE

Example: **VS-800-EGE-AANN-2G45760000**

Revision History		
Date	Approved	Description
03Nov2016	MK	Change the Layout of development specification
02Jun2017	MK, TM	Change from Preliminary version to final version; remove the suggested OE schematic and the pre-production remark for the OE function
15May2018	TM	Update outline drawing & pad layout

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