VS-709
Dual Frequency VCSO

Helping Customers Innovate, Improve & Grow

Description

The VS-709 is a Voltage Controlled SAW Oscillator that operates at the fundamental frequency from one of the two internal SAW filters. The SAW filters are high-Q Quartz devices that enable the circuit to achieve low phase jitter performance over a wide operating temperature range. A divider circuit is deployed for output frequencies less than 600 MHz. The selectable dual oscillator is housed in a hermetically sealed leadless surface mount package and offered on tape and reel. It has a tri-state Frequency Select function that provides one of three conditions: Frequency 1, Output Disable, or Frequency 2.

Features

- Industry Standard Package, 5.0 x 7.0 x 1.8 mm
- 5th Generation ASIC Technology for Ultra Low Jitter
  120 fs-rms (fN = 622.08 MHz, 12 kHz to 20 MHz)
  105 fs-rms (fN = 622.08 MHz, 50 kHz to 80 MHz)
- Output Frequencies from 150 MHz to 1000 MHz
- Spurious Suppression, 90 dBc Typical
- 2.5V or 3.3V Supply Voltage
- LVPECL or LVDS Output Configurations
- Tri-State Frequency Select (F1, OD, F2)
- Compliant to EC RoHS6 Directive

Applications

- PLL circuits for Clock Smoothing and Frequency Translation

Description	Standard
• SONET / SDH	• GR-253-CORE
• OTN (Optical Transport Network)	• ITU-T G.709/Y.1331
• 10 GbE (Gigabit Ethernet)	• IEEE 802.3ae
• 10 GFC (Gigabit Fibre Channel)	• INCITS 364-2003
• 40 GbE & 100 GbE	• IEEE 802.3ba
• Synchronous Ethernet	• ITU-T G.8261
• WiMax	• IEEE 802.16

Block Diagram

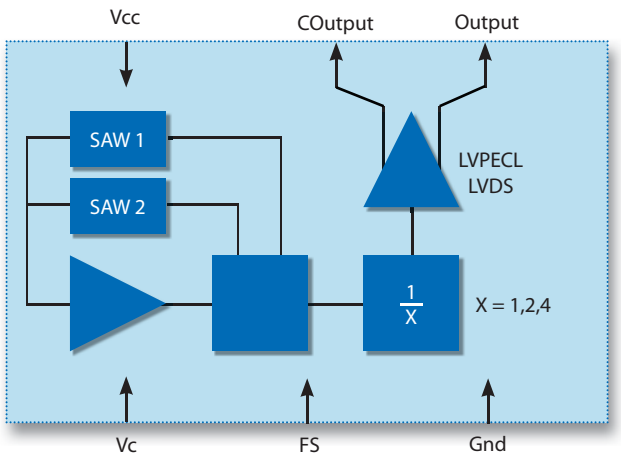

Figure 1. Functional block diagram

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Performance Specifications

Electrical Performance						
Parameter	Symbol	Min	Typical	Maximum	Units	Notes
Frequency						
Nominal Frequency	f_N	150		1000	MHz	1,2,3
Absolute Pull Range	APR	±50			ppm	1,2,3,9
Linearity	Lin		±7		%	2,4,9
Gain Transfer	K_V		+445		ppm/V	2,9
Temperature Stability	f_{STAB}		±100		ppm	1,6
Supply						
Voltage (± 10%)	V_{CC}	2.97	3.3	3.63	V	2,3
Current (Typical 50 Ω Load)	I_{EE}		73		mA	3
Current (No Load)	I_{CC}		60	75	mA	3
Outputs						
Mid Level		V_{CC}-1.5	V_{CC}-1.3	V_{CC}-1.1	mV	2,3
Single Ended Swing			750		mV-pp	2,3
Differential Swing			1.5		V-pp	2,3
Current	I_{OUT}			20	mA	7
Rise Time	t_R		180	250	ps-pp	6,7
Fall Time	t_F		180	250	ps-pp	6,7
Symmetry	SYM	45	50	55	%	2,3
Spurious Suppression (Non-Harmonic)		85	90		dBc	7
Jitter (600 ≤ f_N ≤ 1000)	ΦJ		150		fs-rms	7,8
Jitter (300 ≤ f_N ≤ 500)	ΦJ		190		fs-rms	7,8
Jitter (150 ≤ f_N ≤ 250)	ΦJ		280		fs-rms	7,8
Control Voltage						
Control Voltage	V_C	0.3		3.0	V	3
Input Impedance (F1 or F2 Enabled)	Z_C		123		kΩ	7
Input Impedance (Outputs Disabled)	Z_C		472		kΩ	7
Modulation Bandwidth	BW		200		kHz	7
Operating Temperature	T_{OP}	-40		+85	°C	1,3
Package Size		5.0 x 7.0 x 1.8			mm	

Notes:

1. *See Standard Frequencies and Ordering Information (Pg 8).*
2. *Parameters are tested with production test circuit (Pg 3).*
3. *Parameters are tested at ambient temperature with test limits guard-banded for specified operating temperature.*
4. *Measured as the maximum deviation from the best straight-line fit, per MIL-0-55310.*
5. *The Vc Model is described below (Fig 1).*
6. *Parameters are described with waveform diagram below (Fig 2).*
7. *Not tested in production, guaranteed by design, verified at qualification.*
8. *For Frequencies > 600 MHz, Jitter is integrated across 50 kHz to 80 MHz.*
   For Frequencies < 600 MHz, Jitter is integrated across 12 kHz to 20 MHz. (Both per GR-253-CORE Issue3)
9. *Tested with Vc = 0.3V to 3.0V.*

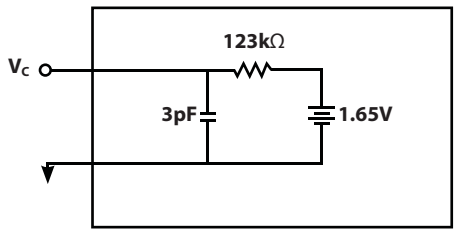


Figure 1. Vc Model - F1 or -F2 Enabled

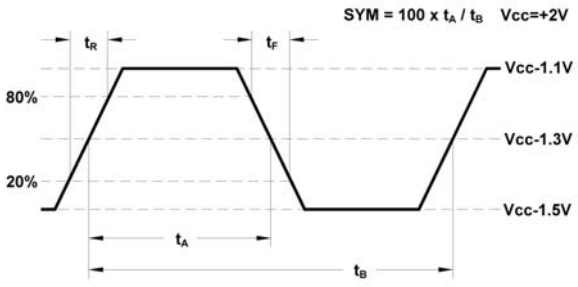


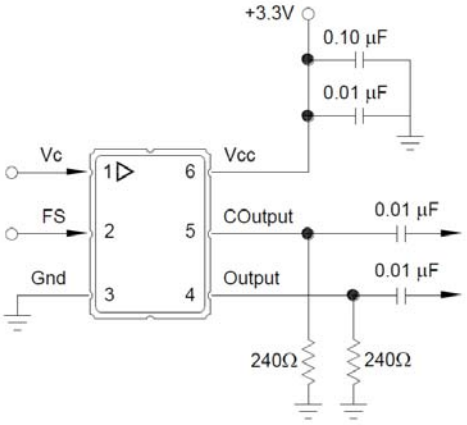
Figure 2. 10K LV-PECL Waveform

Absolute Maximum Ratings

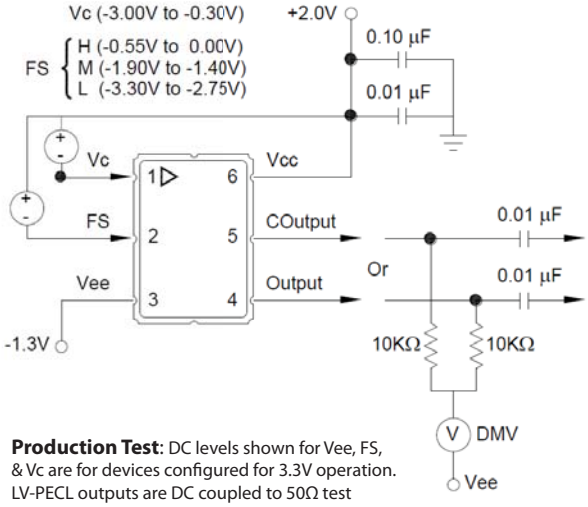
Absolute Maximum Ratings			
Parameter	Symbol	Ratings	Unit
Power Supply	V_{CC}	0 to 6	V
Input Current	I_{IN}	100	mA
Output Current	I_{OUT}	25	mA
Voltage Control Range	V_C	0 to V_{CC}	V
Frequency Select	FS	0 to V_{CC}	V
Storage Temperature	T_{STR}	-55 to 125	ºC
Soldering Temperature/Duration	T_{PEAK}/t_P	260 / 40	ºC/sec

Stresses in excess of the absolute maximum ratings can permanently damage the device. Also, exposure to these absolute maximum ratings for extended periods may adversely affect device reliability. Functional operation is not implied at these or any other conditions in excess of those represented in the operational sections of this datasheet. Permanent damage is also possible if any device input (Vc or FS) draws >100 mA.

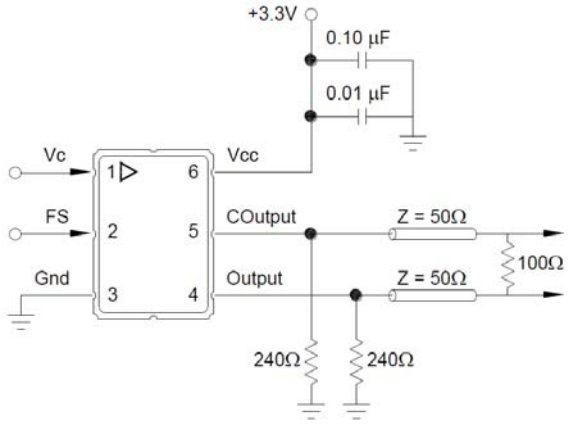
Test Circuits & Output Load Configurations



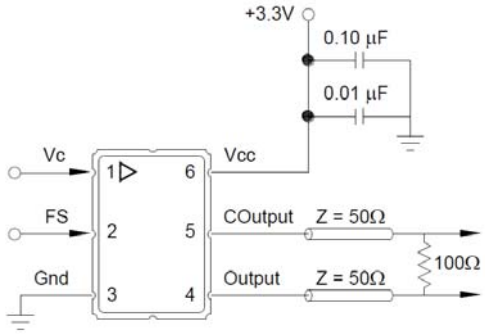
Functional Test: Allows use of standard power supply biasing configuration. Pull down resistors are used for LV-PECL outputs and are removed for with LVDS outputs. Since the LVDS outputs are AC coupled, the output DC levels cannot be measured.



Production Test: DC levels shown for Vee, FS, & Vc are for devices configured for 3.3V operation. LV-PECL outputs are DC coupled to 50Ω test equipment. LVDS outputs are connected to a digital volt meter, then AC coupled to the test equipment. The digitial volt meter allows for Mid Level & Swing measurements.

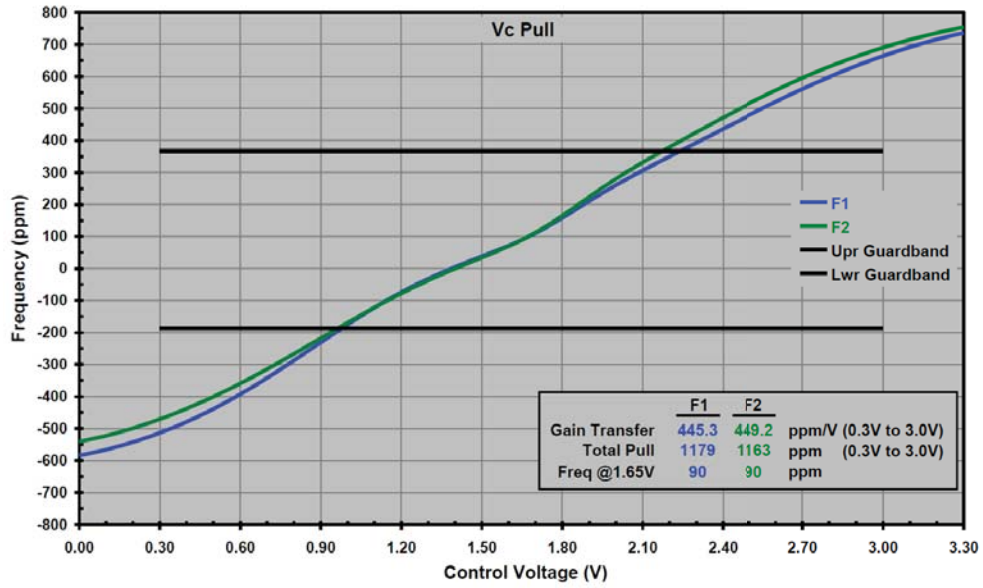


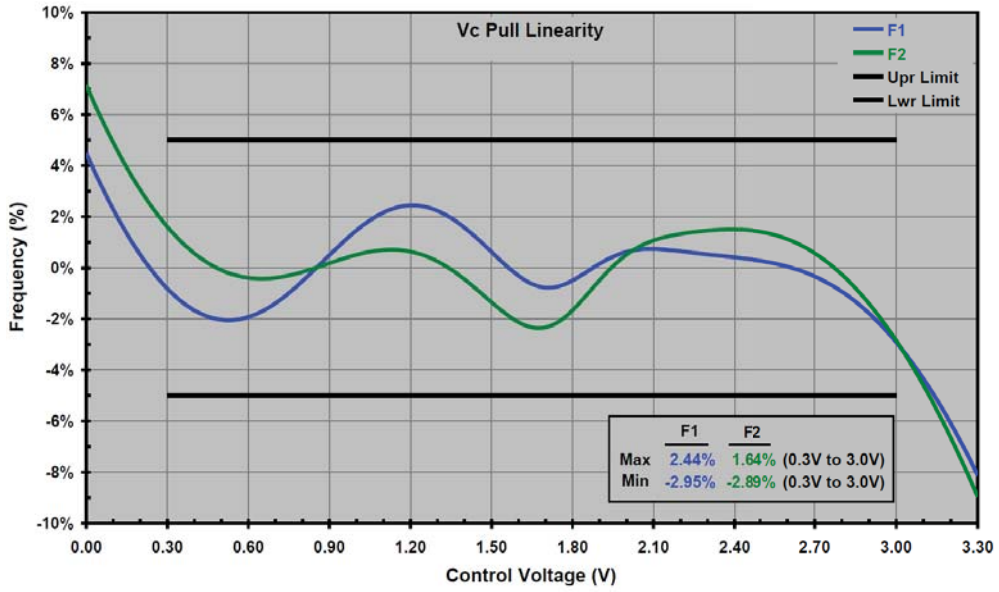
LV-PECL to LV-PECL: For short transmission lengths, the pulldown resistor values shown provide reasonable powerconsumption and waveform performance.

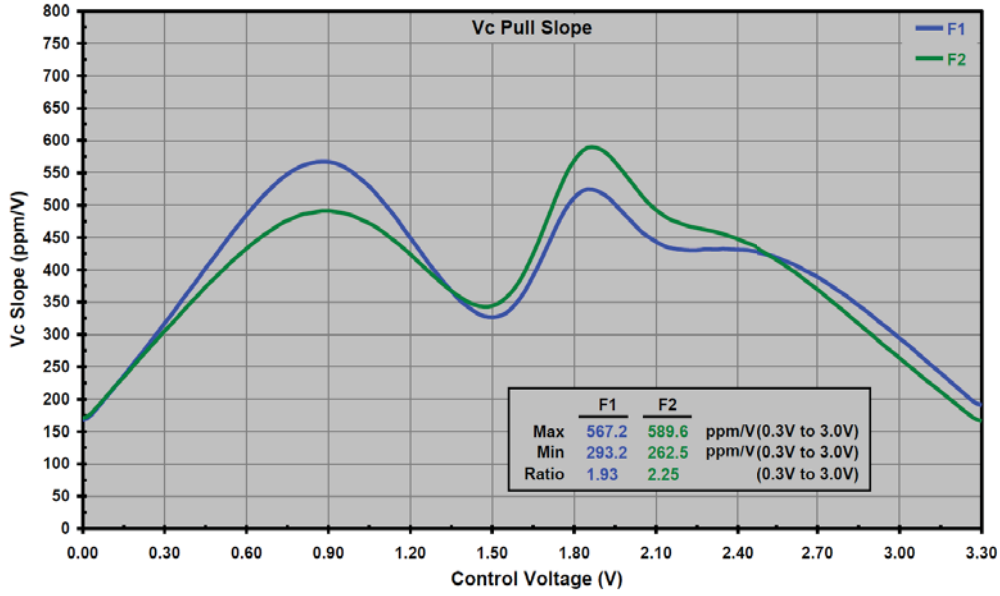


LVDS to LVDS: The 100Ω resistor should be removed if this load isprovided internally within the LVDS receiver.

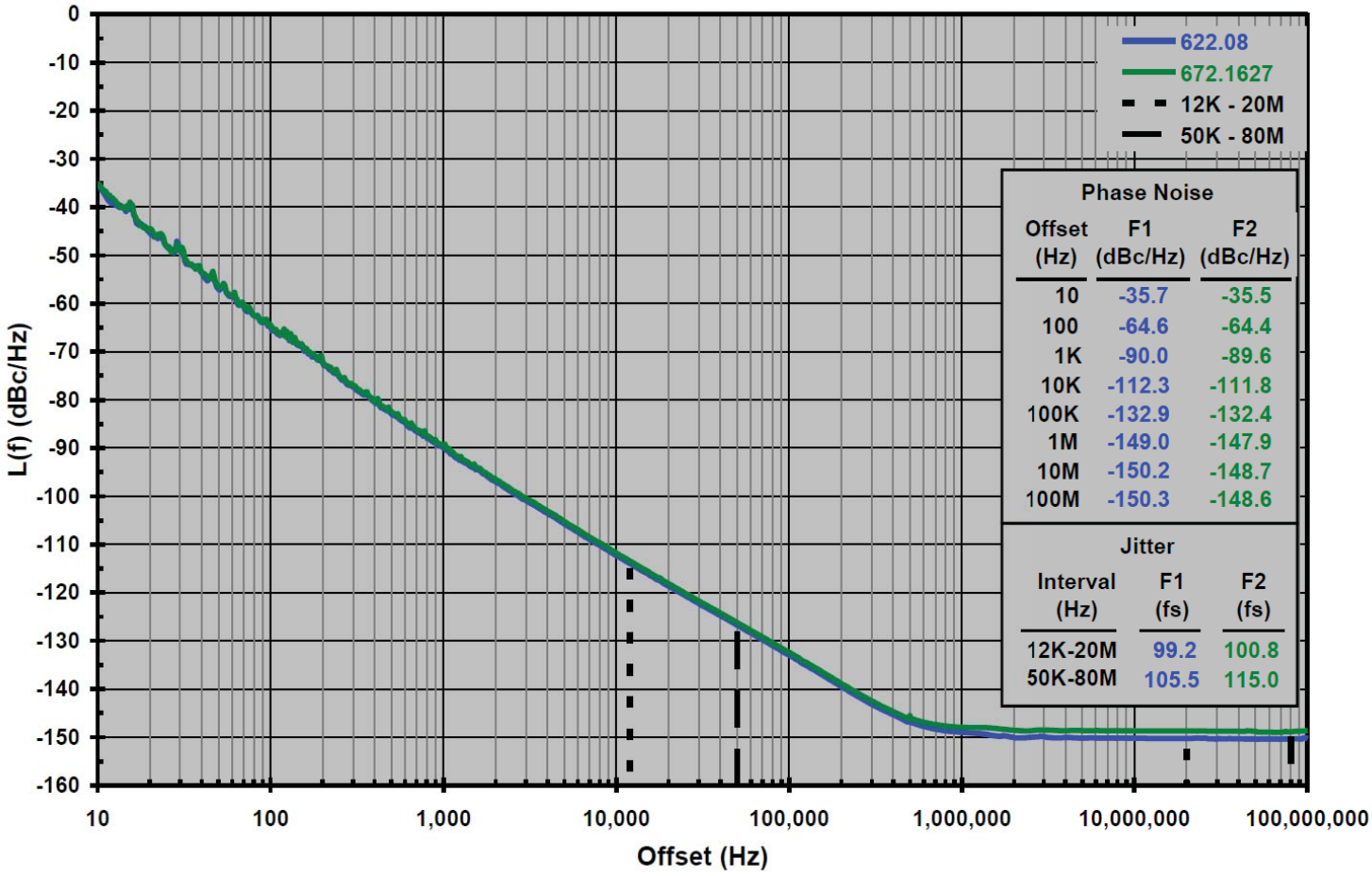
Typical Characteristics: Vc Pull, Vc Pull Linearity, & Vc Pull Slope







Typical Characteristics: Phase Noise & Jitter



	F1	F2	F1	F2	F1	F2	F1	F2	
PN / Jitter	622.08	669.33	644.53	698.81	657.42	707.35	718.86	909.71	Units
L (f) @ 10	-32.9	-33.6	-36.1	-34.6	-33.1	-32.2	-31.9	-31.6	dBc/Hz
L (f) @ 100	-62.6	-62.6	-64.6	-63.6	-62.0	-61.4	-62.0	-60.2	dBc/Hz
L (f) @ 1K	-88.4	-88.1	-90.2	-89.2	-88.4	-87.6	-87.0	-84.7	dBc/Hz
L (f) @ 10K	-111.1	-110.7	-112.1	-111.2	-111.0	-110.0	-109.0	-106.3	dBc/Hz
L (f) @ 100K	-132.2	-131.8	-132.6	-131.7	-132.0	-131.0	-129.6	-126.8	dBc/Hz
L (f) @ 1M	-148.8	-147.6	-149.0	-147.4	-148.5	-147.0	-148.0	-144.6	dBc/Hz
L (f) @ 10M	-149.9	-148.3	-150.2	-147.9	-149.7	-147.2	-149.3	-144.0	dBc/Hz
L (f) @ 100M	-149.9	-148.4	-150.5	-147.6	-149.8	-147.4	-148.8	-144.2	dBc/Hz
12K - 20M	111.2	112.7	98.0	104.2	107.9	115.7	120.3	138.3	fs-rms
50K - 80M	110.7	121.1	100.9	119.6	106.5	120.0	108.1	147.6	fs-rms

Reliability

VI qualification includes aging at various extreme temperatures, shock and vibration, temperature cycling, and IR reflow simulation. The VS-709 family is capable of meeting the following qualification tests:

Environmental Compliance	
Parameter	**Conditions**
Mechanical Shock	MIL-STD-883, Method 2002 B
Mechanical Vibration	MIL-STD-883, Method 2007 A
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2016
Moisture Sensitivity Level	IPC/JEDEC J-STD-020, MSL1

Handling Precautions

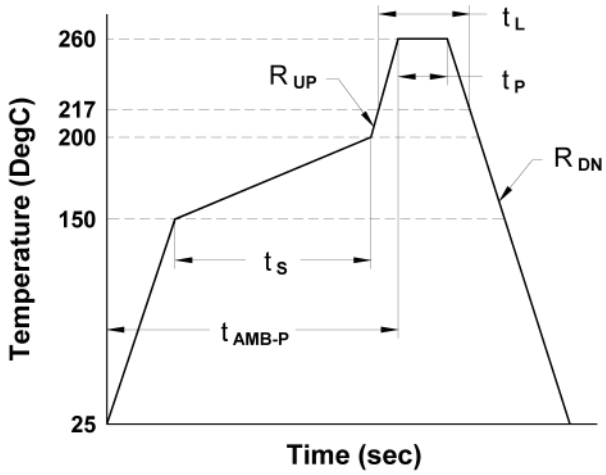
Although ESD protection circuitry has been designed into the VS-709 proper precautions should be taken when handling and mounting. VI employs a human body model (HBM) and a charged-device model (CDM) for ESD susceptibility testing and design protection evaluation.

ESD Ratings		
Model	**Minimum**	**Conditions**
Human Body Model	2000 V	MIL-STD 883, Method 3015
Charged Device Model	1000 V	JEDEC, JESD22-C101
Machine Model	200 V	JEDEC, JESD22-A115-A

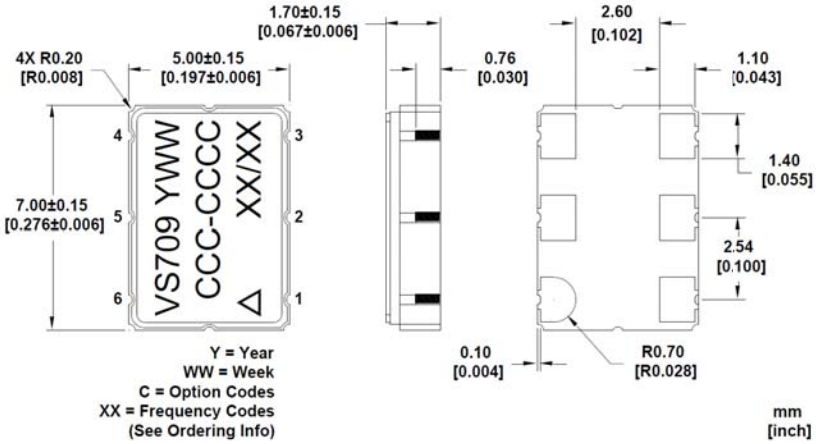
Reflow Profile (IPC/JEDEC J-STD-020)		
Parameter	**Symbol**	**Value**
PreHeat Time	t_S	60 s min., 180 s max.
Ramp Up	R_{UP}	3°C / s max.
Time Above 217°C	t_L	60 s min., 150 s max.
Time To Peak Temperature	t_{AMB-P}	480 s max.
Time At 260°C	t_P	20 s min., 40 s max.
Ramp Down	R_{DN}	6°C / s max.

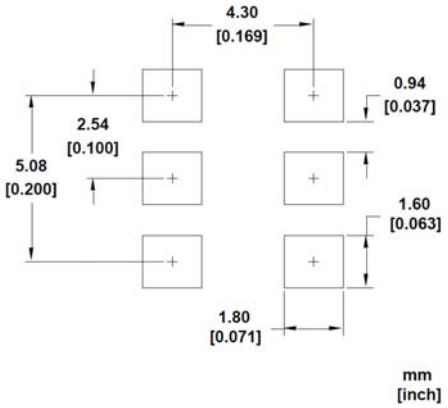
The VS-709 is qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The temperatures refer to the topside of the package, measured on the package body surface. The VS-709 device is hermetically sealed so an aqueous wash is not an issue.

Terminal Plating: Electroless Au > 1.50 µm over
Electroless Ni > 1.90 µm



Outline Drawing & Pad Layout



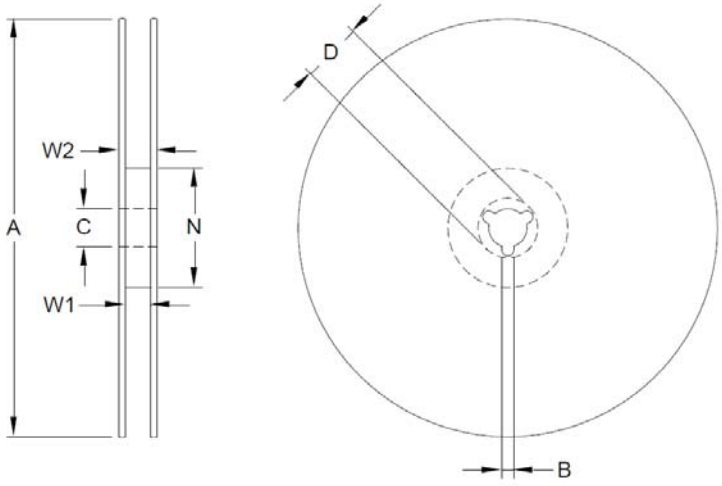


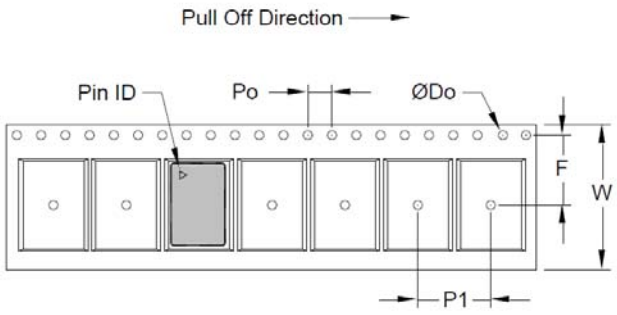
Pin Out		
Pin	**Symbol**	**Function**
1	V_C	Control Voltage
2	FS	Frequency Select
3	GND	Case and Electrical Ground
4	Output	Output
5	COutput	Complementary Output
6	V_{CC}	Power Supply Voltage

Frequency Select (Tri-State LV-CMOS)		
FS	**Voltage Range**	**Result**
H	($5V_{CC}$ / 6) to V_{CC}	F2
M	(V_{CC} / 2) ± 15%(V_{CC} / 2)	OD
L	Gnd to (V_{CC} / 6)	F1

LV-CMOS Tri-State Control
Floating FS Results in OD

Tape and Reel (EIA-481-2-A)





Tape Dimensions (mm)						Reel Dimensions (mm)							
Dimension	**W**	**F**	**Do**	**Po**	**P1**	**A**	**B**	**C**	**D**	**N**	**W1**	**W2**	**#Per Reel**
Tolerance	**Typ.**	**Typ.**	**Typ.**	**Typ.**	**Typ.**	**Typ.**	**Min.**	**Typ.**	**Min.**	**Min.**	**Typ.**	**Max.**	
VS-709	16	7.5	1.5	4	8	178	1.5	13	20.2	50	16.4	22.4	200

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Ordering Information

Standard Frequencies (MHz)						
155.520000 **M2**	156.250000 **M3**	161.132813 **M4**	166.628572 **M5**	167.331646 **N2**	168.040678 **N3**	173.370748 **ND**
184.320000 **NH**	307.200000 **RX**	311.040000 **P1**	368.640000 **RY**	614.400000 **RG**	622.080000 **P2**	625.000000 **P3**
644.531250 **P4**	657.421875 **PB**	666.514286 **P5**	669.326582 **R3**	672.162712 **R5**	690.569196 **R4**	693.482991 **R6**
696.421478 **V1**	696.614900 **V8**	697.500000 **VV**	698.812330 **VC**	699.426250 **VM**	700.000000 **W6**	707.352650 **TC**
718.863800 **V6**	737.280000 **TL**	753.621100 **VN**	753.800000 **W7**	780.500000 **W8**	781.025550 **VR**	794.727800 **VP**
802.500000 **VW**	873.515414 **WJ**	905.499558 **V7**	993.409500 **WK**			

Other Frequencies Available Upon Request.
Frequency F1 Must Be Lower Than Frequency F2.
Frequencies F1 & F2 Must Be Selected Within One Frequency Range: (150 - 250), (300 - 500), (600 - 1000) [MHz]

Ordering Information

VS- 709 - E C E - K A A N - P2 / P4

Product Family
VS: VCSO

Package
709: 5.0 x 7.0 x 1.8mm

Input
E: 3.3 V
H: 2.5 V

Output
C: LVPECL
D: LVDS

Operating Temperature
E: -40 to 85°C

Absolute Pull Range
K: ± 50 ppm
S: ± 100 ppm
T: ± 120 ppm

Enable Logic (Float Condition)
A: L=F1, M=OD, H=F2

Oscillator Gain
A: Standard
B: Low

Factory Use
N: N/A

Frequency 1
See Above

Frequency 2
See Above

Example1: VS-709-ECE-KAAN-M2/NH
Example2: VS-709-EDE-SAAN-R3/R4

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Revision History		
Date	**Approved**	**Description**
30Jul2008	JM, BW	Preliminary Release.
09Jan2009	BW	Supply voltage, output type, operating temperature codes changed to universal part number codes.
30Jan2009	JM	New rendering, phase noise plot, additional freq code.
05Nov2009	BW	Additional frequency codes added.
24Feb2010	JM	Rendering, outline, & order info modified to show "/" between F1 and F2. Updated frequency codes. New Vc Pull & Phase Noise Plots.
08Mar2010	JM	Modified Jitter Note 8 on Pg2 for frequencies < 600 MHz. Updated Vc Pull Plots.
23Mar2010	BW	Official Release.
08Aug2011	JM	Corrected production test notes on Pg3. Corrected contact phone numbers, added ±120 ppm APR order option and frequency codes (VC,VM,VN,VP,VR,VV,VW) on Pg8.
22Mar2012	JM	Added Phase Noise / Jitter Table on Pg5.
08Aug2012	BW	Added following frequency codes (W6, W7, W8) on Pg8.
02Dec2013	TM, MK	Added following frequency codes (WJ, WK) on Pg8. Added Address for Teltow
02Mar2014	MK	Vectron Logo changed, Vectron Address Shanghai changed

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