FMA3051

Pilot Datasheet v2.1

12.5-15.5 GHz MMIC High Power Amplifier

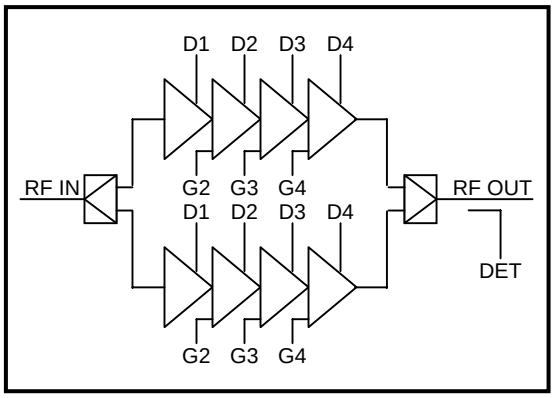
Features

- 35 dB Gain
- 30 dBm P_{1dB} Output Power at 6 V, 1.2 A
- 40 dBm OIP3
- pHEMT Technology
- On-chip output power detector
- 5 x 3 sq. mm die

General Description

The FMA3051 is a high performance 12.5-15.5 GHz Gallium Arsenide monolithic amplifier. It is suitable for use in point-to-multipoint communications, sat-com and electronic warfare applications. The die is fabricated using the Filtronic 0.25 µm process. The balanced design offers high output power with low return losses. Power detection is achieved with an on-chip coupled detector associated with diode reference voltage. The circuit is DC blocked at both the RF input and the RF output.

Functional Schematic



Typical Applications

- Point-to-point radio
- Point-to-multipoint radio
- Sat-com
- Electronic Warfare

Electrical Specifications

Parameter	Conditions	Min	Typ	Max	Units
Small Signal Gain	12.5-15.5 GHz, Vd = 6 V, 1200 mA	32	35	36	dB
Input Return Loss	12.5-15.5 GHz, Vd = 6 V, 1200 mA		-12	-10	dB
Output Return Loss	12.5-15.5 GHz, Vd = 6 V, 1200 mA		-15	-12	dB
Output Power at 1dB compression point	12.5-15.5 GHz, Vd = 6 V, 1200 mA	30	33	35	dBm
Output IP3	12.5-15.5 GHz, Vd = 6 V, 1200 mA		40		dBm
Drain Current	6.0 V	800	1100	1400	mA
Typical gate voltage		-0.5	-0.4	-0.3	V

Note: $T_{AMBIENT}$ = +25°C, Z_0 = 50Ω
Performance for on-wafer measurements

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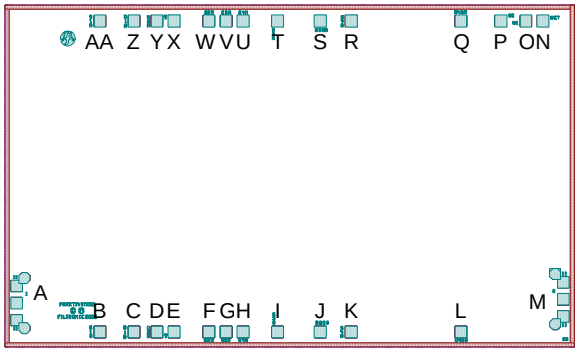
Absolute Maximum Ratings:

Parameter	Symbol	Absolute Maximum
Max Input Power	Pin	+20dBm
Drain Voltage	VDD	+10V
Operating Temp	Toper	-40°C to +85°C
Storage Temp	Tstor	-55°C to +150°C

Note: Exceeding any one of these absolute maximum ratings may cause permanent damage to the device.

Pad Layout:



Pad Ref	Pad Name	Description
A	IN	RF in
B	S1B	GND
C	D1B	Vd1 bias south
D	D2B	Vd2 bias south
E	S2B	GND
F	G2B	Vg2 bias south
G	G3B	Vg3 bias south
H	G4B	Vg4 bias south
I	S3B	GND
J	D3BB	Vd3 bias south
K	S4B	GND
L	D4BB	Vd4 bias south
M	OUT	RF out
N	DET	Detected power voltage
O	Q1	Reference voltage for diode detector
P	S5	GND
Q	D4BA	Vd4 bias north
R	S4A	GND
S	D3BA	Vd3 bias north
T	S3A	GND
U	G4A	Vg4 bias north
V	G3A	Vg3 bias north
W	G2A	Vg2 bias north
X	S2A	GND
Y	D2A	Vd2 bias north
Z	D1A	Vd1 bias north
AA	S1A	GND

Die Size (µm)	Die Thickness (µm)	Min. Bond Pad Pitch (µm)	Min. Bond pad Opening (µm x µm)
5100 x 3000	100	150	92 x 92

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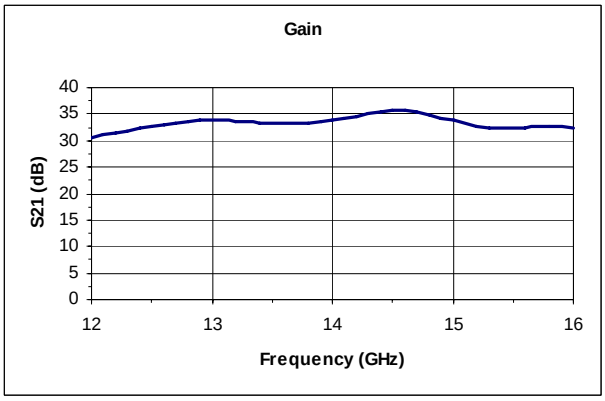
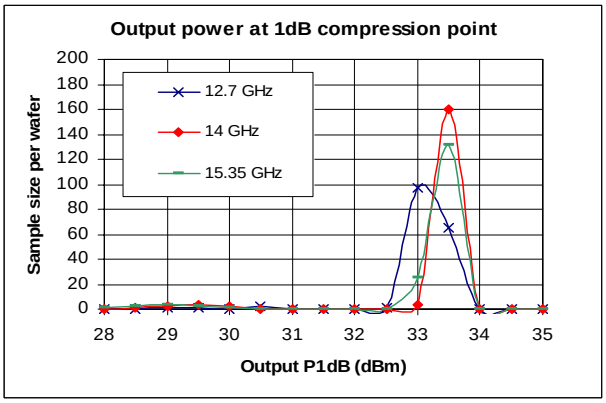
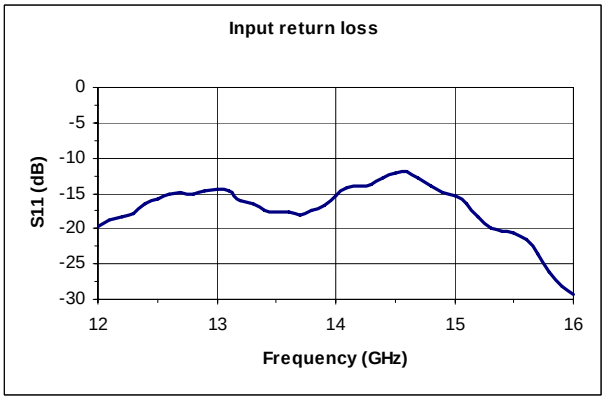
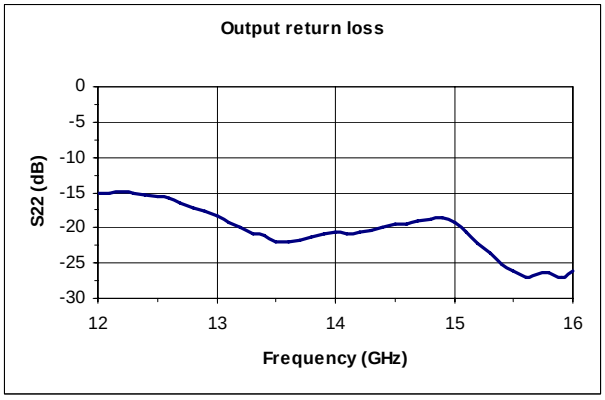
TYPICAL PERFORMANCE FOR ON-WAFER MEASUREMENTS:

Note: Measurement Conditions I_D = 1100 mA, V_{DD} = 6V, $T_{AMBIENT}$ = 25°C.









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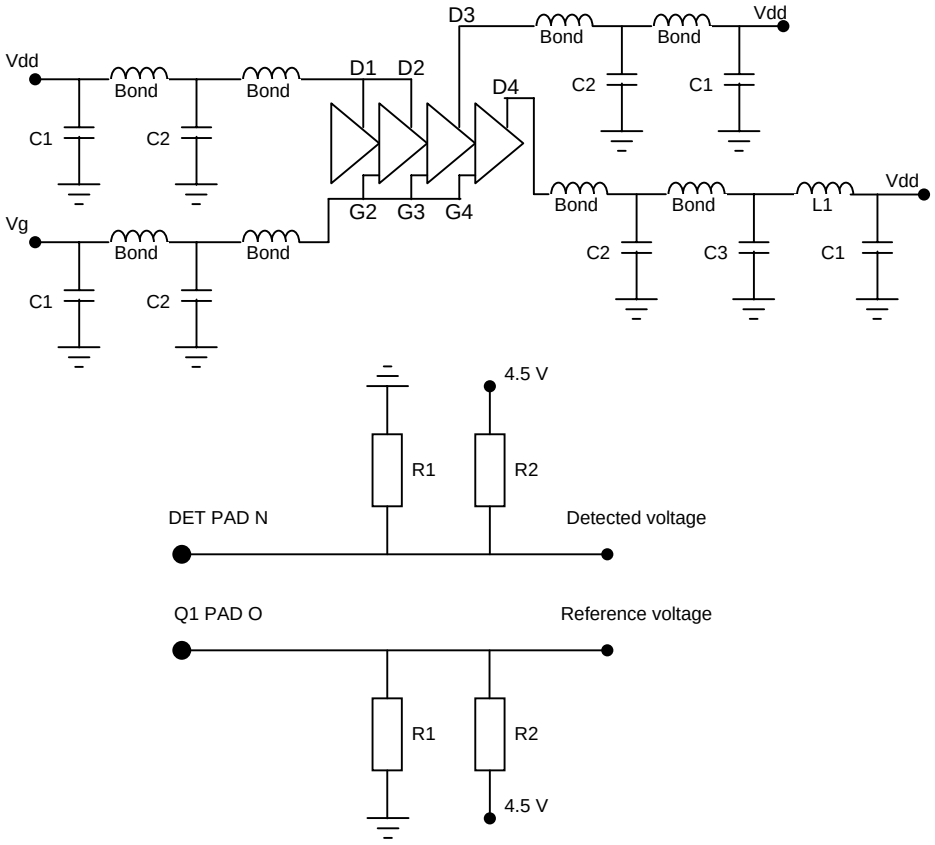
BIASING CIRCUIT SCHEMATIC:

North and South are biased separately, only one side is represented. Please refer to the Assembly diagram below for surface mount components locations.



REFERENCE	COMPONENT DESCRIPTION	QUANTITY
C1	Capacitor, 100 nF, surface mount 0402	8
C2	Capacitor, 100 pF, single layer, to epoxy in cavity	8
C3	Capacitor, 10 nF, surface mount 0402	2
L1	Inductor, 10 nH, surface mount 0402	2
Bond	Bondwire	–
R1	Resistor, 1 kΩ, surface mount 0402	2
R2	Resistor, 1.5 kΩ, surface mount 0402	2

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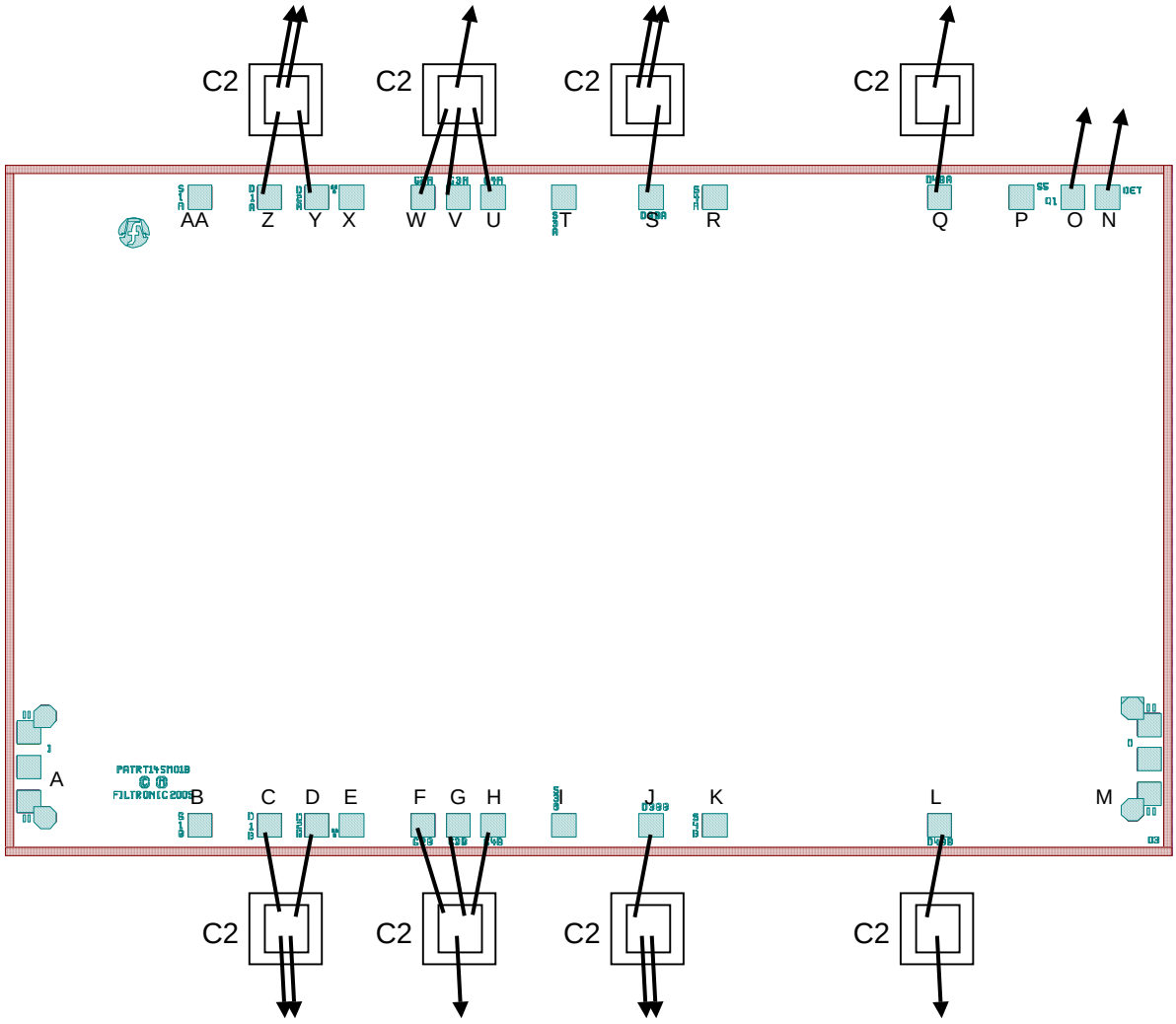
ASSEMBLY DIAGRAM

It is recommended that the RF connections be made using bond wires with 25µm diameter and a maximum length of 300µm.



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Preferred Assembly Instructions:

GaAs devices are fragile and should be handled with great care. Specially designed collets should be used where possible.

The recommended die attach is gold/tin eutectic solder under a nitrogen atmosphere. Stage temperature should be 280-290°C; maximum time at temperature is one minute. The recommended wire bond method is thermo-compression wedge bonding with 0.7 or 1.0 mil (0.018 or 0.025 mm) gold wire. Stage temperature should be 250-260°C.

Bonds should be made from the die first and then to the mounting substrate or package. The physical length of the bondwires should be minimised especially when making RF or ground connections.

Handling Precautions:

To avoid damage to the devices care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. These devices should be treated as Class 0 (0-250 V) as defined in JEDEC Standard No. 22-A114. Further information on ESD control measures can be found in MIL-STD-1686 and MIL-HDBK-263.

Application Notes & Design Data:

Application Notes and design data including S-parameters are available on request.

Disclaimers:

This product is not designed for use in any space based or life sustaining/supporting equipment.

Ordering Information:

Part Number	Description
FMA3051-000	Die in Waffle-pack (Gel-pak available on request)

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