The TriQuint TGS23xx series of GaN switches offers high power handling and fast switching speeds. To realize the high power handling capability, large negative voltages are used to control the device, posing a challenge to driver design providing the required control voltages.

Switch Driver 1:

Fig. 1 is a low cost circuit that will switch rapidly where bypass capacitors on the control lines are omitted. It can also be employed for the case where speed is not critical in a bypassed circuit. The equivalent internal circuit of the TGS23XX GaN Switch is 14.5 K in series driving 0.8pF capacitance in shunt to ground. Given the sub 50 nS delay times for the PNP switching elements, the circuit switches in the hundreds of nS range. Adding control line bypass capacitance slows the circuit down in asymmetric fashion as shown in **Fig 2.** While the rising transition from –V- to 0V is relatively fast due to the low impedance FET Q1, the falling transition from 0V to V- is now dominated by the RC time constant, under 10 uS range with 100pF bypass caps and 15k pull down resistors. Low cost commodity components are specified throughout the design. The control voltage must be referenced to the V+ supply. As a result, the negative voltage can be varied over the -10 to -40 V range without any circuit changes. The dual transistors are not critical, and can be selected by insuring sufficient margin between the device Vceo maximum rating specification and the switch bias voltage V-.

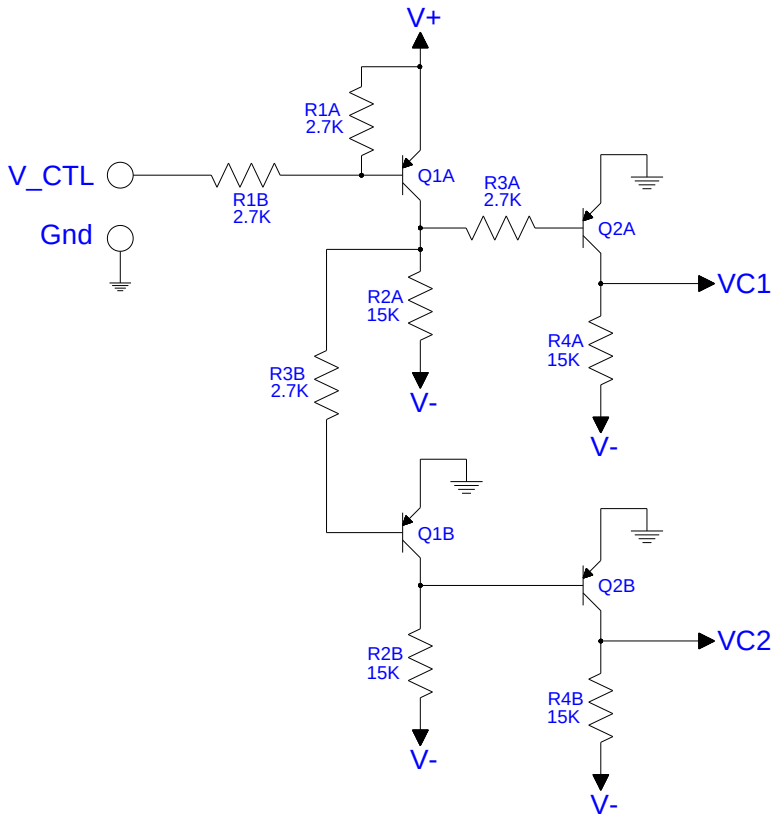

Fig. 1 Low Cost GaN SPDT Switch Driver. Q1 and Q2 are MDT2907A, MMDT5401 in 40Vdesigns, MMDT3906 useable at lower voltages.

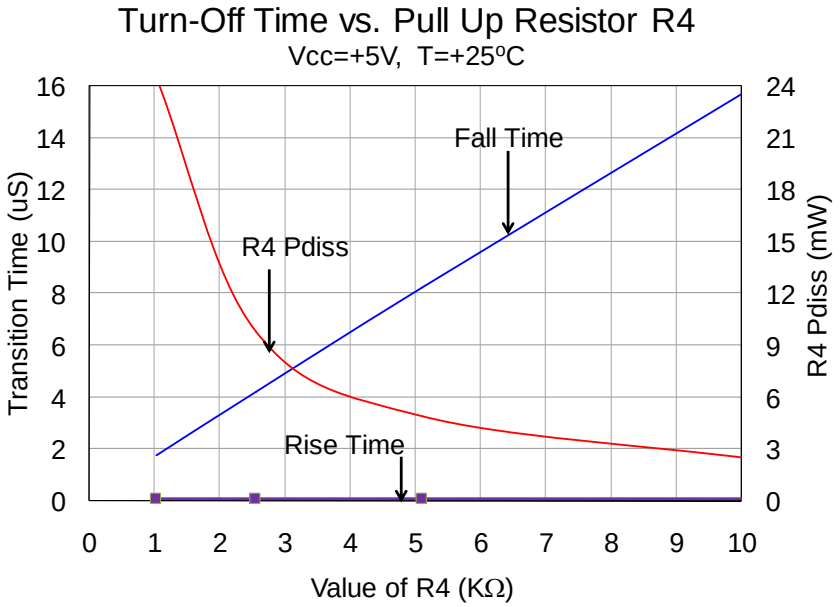

Fig. 2 Open Collector Rise and Fall Times. Bypass Capacitance approx.560 pF. Power dissipation curve assumes V- = 5V.

Switch Driver 2:

Zener diodes can also be used for the logic level translation. **Fig. 3** is a low cost design that uses Zener diodes to level shift the logic control voltage to MOSFET switching elements. While the dual inverter gate operates from 2.7…5.0V, the Zener diode voltage of D1 needs to be selected to be the same as the positive supply voltage for the logic. In **Fig. 3** the 5V logic supply requires the specified 5.1V Zener diode for level translation. In order to prevent negative voltage from appearing at the output of the inverters, the negative voltage applied to the level shifters must also equal the positive supply voltage. Once +/-5V is set on the circuit, the negative switch bias V- can be set anywhere in the -10 V to -40V range. Switching speeds are similar to the bipolar design. Without capacitance on the control lines, the circuit provides 35nS rise and fall times. As a result, It will turn the TriQuint GaN switch TGS2351 on and off within 50nS, as shown in **Fig. 4**.

Watch out for the power dissipation of the pull down resistors. They must be able to dissipate current generated by the negative bias voltage V-. For typical 0805 or 0603 sized resistors, values in the 10K to 30K range are common, depending on the exact V- applied to the circuit.

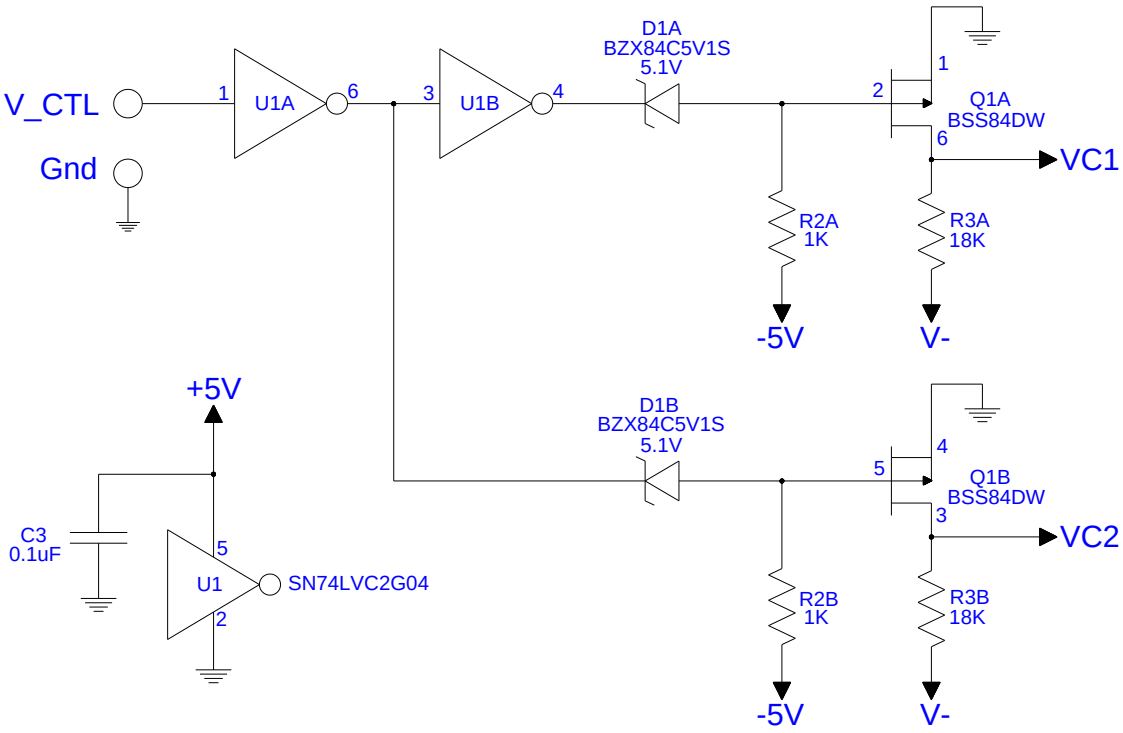

Fig. 3 Low Cost GaN SPDT Switch Driver using MOSFET Switching and Zener diode level translation. Using dual components throughout the design keeps the BOM count down to 6 parts.

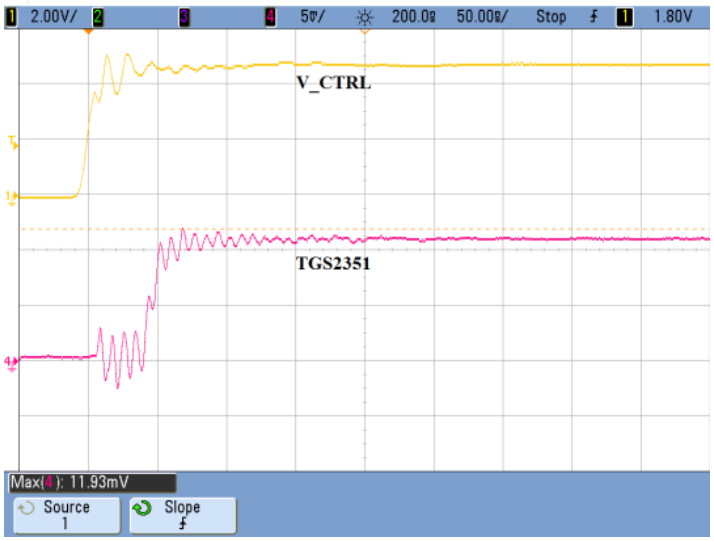

Fig. 4 FET based driver circuit (Fig. 3) turns GaN Switching TGS2351 on and Off within 50 nS.

Switch Driver 3:

Fig. 5 is a schematic of a driver circuit that can drive high capacitive loads due to bypass capacitors at very fast speeds. Each output transistor has a high speed complementary driver on its base to switch as fast as possible. To avoid the condition where both output transistors are conducting simultaneously, U1 and U2, along with R1 & C1, form a break-before-make generator. The PNP transistor Q3A is turned off about 50 ns before the lower NPN transistor Q3B is activated. Likewise the lower NPN device Q3B is turned off about 50 ns before the upper PNP transistor Q3A. The devices are both DC coupled ON, with AC coupled signals quickly shutting the devices OFF. With a 100 pF load, the circuit provides 30 nS rise and fall time with 120 nS delay, as shown in **Fig. 6**. The 15K has been selected to allow for operation from -10V to -40V, while the 2.7K allows operation from 1.65 to 5 V. Given fixed supply voltages, these values can be optimized for power dissipation.

In the lab often there is the possibility of live probing or shorting at the driver outputs. Additional protection resistors may be added in series with either the collector of the output devices, or on the control lines themselves, where added series resistors could also double as RF isolation when located near the device. These protection measures will be at the expense of speed, particularly for the high speed driver circuit.

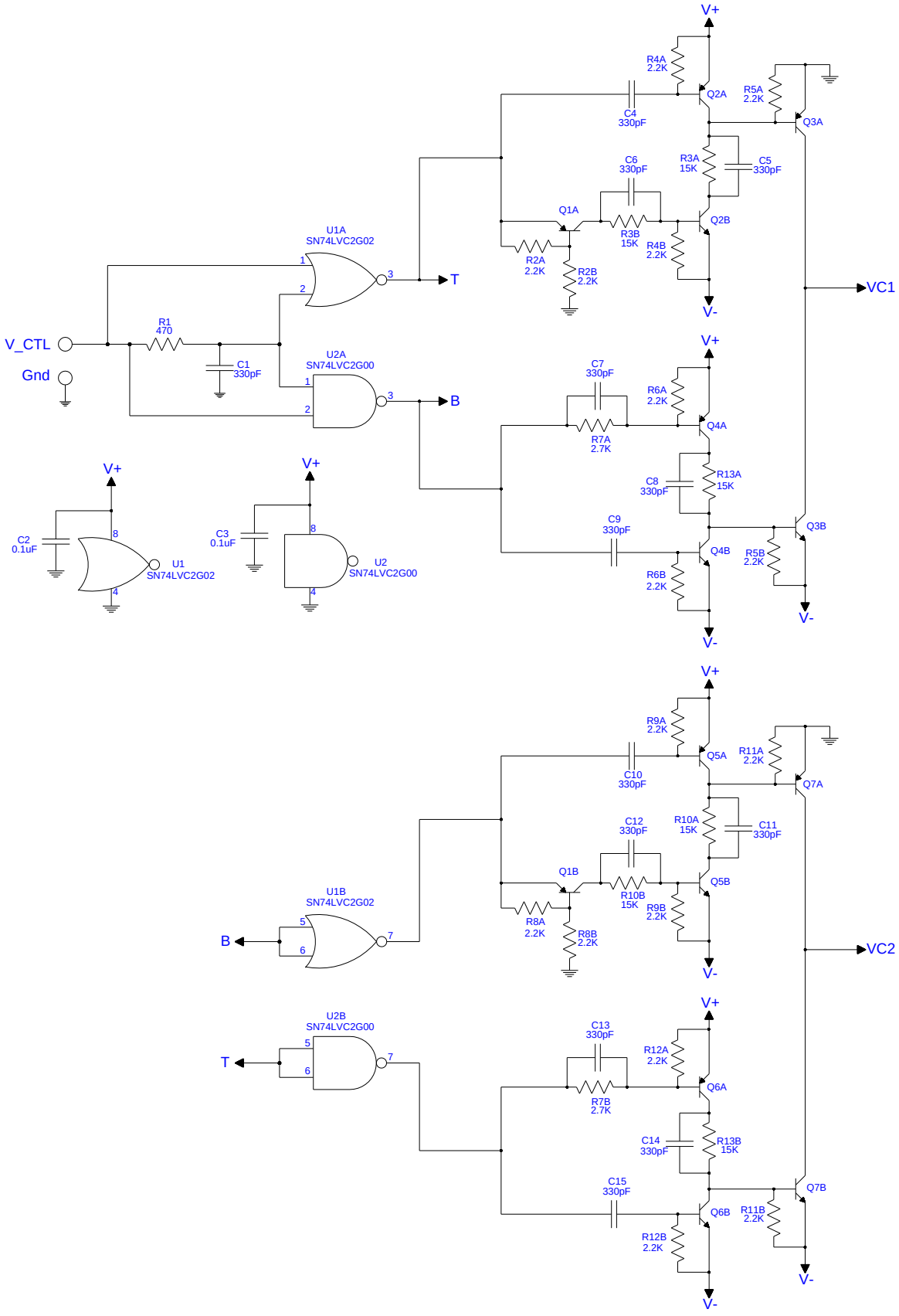

Fig. 5 High Speed GaN SPDT Switch Driver for driving high

bypass capacitive loads.

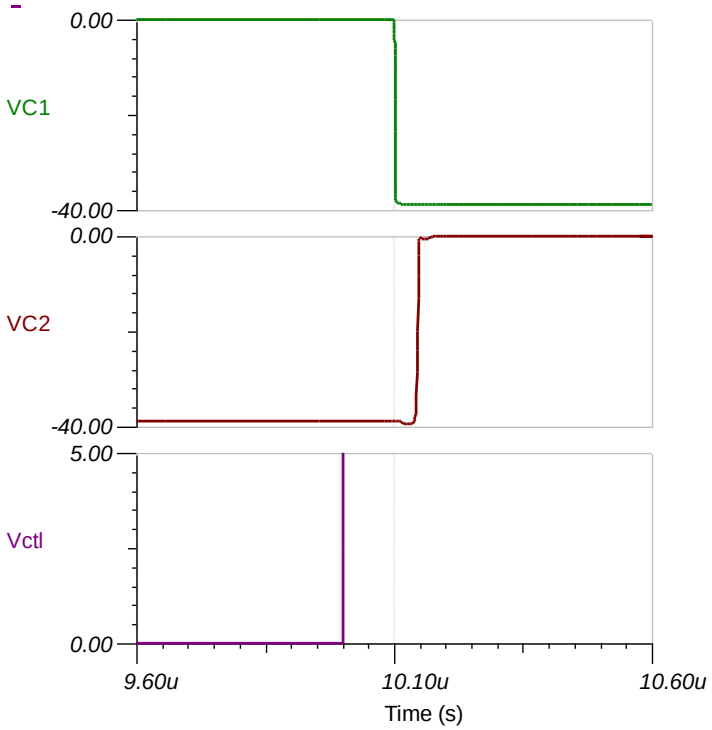

Fig. 6 Switching Speed Simulation for the High Speed GaN SPDT Switch Driver. Delay time is 120 nS, with the delay between the two control signals offset by the delay of inverters U1B & U2B. Rise and fall times are 35 nS typical. Analysis assumes control line bypass capacitance of 100pF.

The NPN and PNP devices are inexpensive dual SOT-363 surface mount devices. For -20V applications the MMDT2227 or equivalent device is recommended. For applications up to -40 V the higher voltage HBDM60V600W or equivalent is required. Speed up capacitors C5 – C8 and C11 – C14 may be omitted if switching speeds of several hundred nanoseconds is acceptable.

The BOM is kept to a minimum by using dual devices and passives through the design. **Table 1** lists the components. The design is insensitive to component values and a wide range of values will work, making it easy to pick out values already found on existing assembly BOMs.

TABLE 1: BOM FOR HIGH SPEED DRIVER

Ref. Desg	Value	Description	Mfg P/N
U1		Dual NOR	SN74LCV02
U2		Dual NAND	SN74LVC00
Q1		Dual PNP	MMDT5401A
Q2 – Q7		PNP + NPN	HBDM60V600W
C2, C3	0.1 uF	Cap., 0402, X7R 10%	various
C1, C3 – C15	330 pF	Cap., 0402, X7R 10%	various
R1	470 Ω	Res., 0402, 5%	various
R2, R4, R5, R6, R8, R9, R11, R12,	2.2K	Res., Dual Array, 0402, 5%	various

R7	2.7K	Res., Dual Array, 0402, 5%	various
R3, R10, R13	15K	Res., Dual Array, 0402, 5%	various