Description

The SiT5541 is a Stratum 3E MEMS precision oscillator optimized for ±10 ppb stability from -40°C to 85°C. It also supports ±20 ppb stability in a wider temperature range (down to -40°C and up to 105°C). Engineered for exceptional dynamic performance, it is ideal for replacing larger and less robust quartz OCXOs. SiT5541 is uniquely positioned for high highly accurate aerospace and defense applications.

Leveraging SiTime's unique DualMEMS™ temperature sensing and TurboCompensation™ technologies, the SiT5541 delivers the best dynamic performance for timing stability in the presence of environmental stressors such as air flow, temperature perturbation, vibration, shock, and electromagnetic interference. This device also integrates multiple on-chip regulators to filter power supply noise, eliminating the need for a dedicated external LDO.

The SiT5541 can be factory programmed for any combination of voltage, and pull range. Programmability enables designers to optimize clock configurations while eliminating long lead times and customization costs associated with quartz devices where each frequency is custom built.

Refer to Manufacturing Guideline for proper reflow profile and PCB cleaning recommendations to ensure best performance.

Features

- Any frequency from 1 MHz to 60 MHz in 1 Hz steps
- Factory programmable options for low lead time
- Best dynamic stability under airflow, thermal shock
  - ±10 ppb stability over temperature: -40°C to 85°C
  - ±0.5 ppb/°C typical frequency slope (ΔF/ΔT)
  - 2e-11 ADEV at 10 second averaging time
- No activity dips or micro jumps
- Resistant to shock, vibration and board bending
- On-chip regulators eliminate the need for external LDOs
- 2.5 V, 2.8 V, 3.0 V and 3.3 V supply voltage
- LVCMOS or clipped sinewave output
- RoHS and REACH compliant
- Pb-free, Halogen-free, Antimony-free
- 7.0 mm x 5.0 mm ceramic package
- Contact SiTime for tighter stability, wider temperature, and alternate package options

Applications

- Ruggedized communication networks
- SATCOM
- Military portable radios
- GPS/GNSS timing
- Military, defense, space, avionics systems

Block Diagram

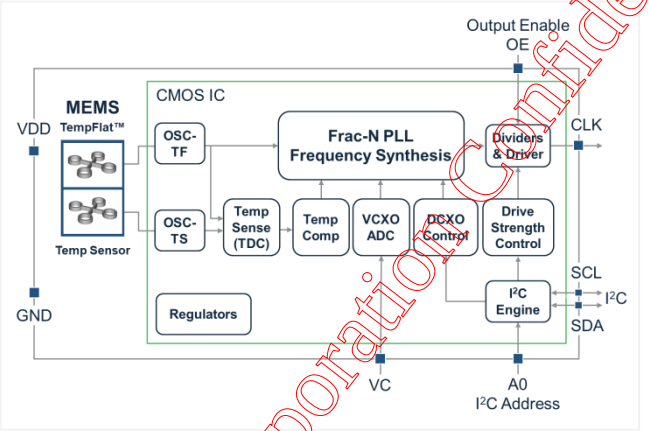


Figure 1. SiT5541 Block Diagram

7.0 mm x 5.0 mm Package Pinout

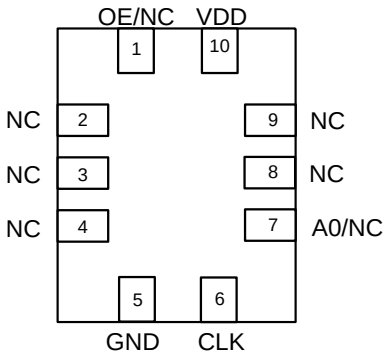
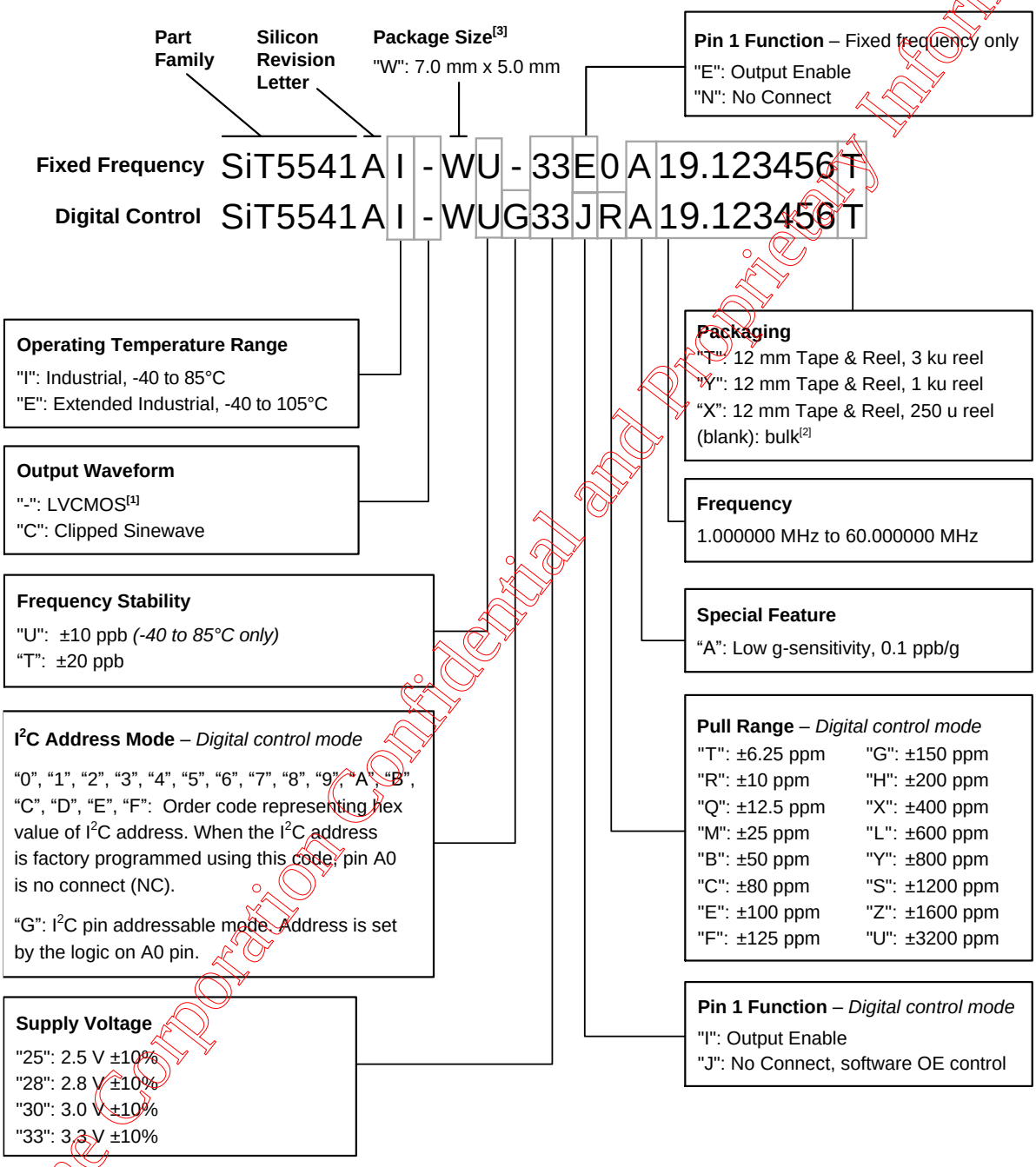


Figure 2. Pin Assignments (Top view)

Ordering Information

The part number guide illustrated below is for reference only, in which boxes identify order codes having more than one option. To customize and build an exact part number, use the SiTime Part Number Generator. To validate the part number, use the SiTime Part Number Decoder.



Notes:

1. "-" corresponds to the default rise/fall time for LVCMOS output as specified in Table 1 (Electrical Characteristics). Contact SiTime for other rise/fall time options for best EMI or driving multiple loads. For differential outputs, contact SiTime.
2. Bulk is available for sampling only.
3. Contact SiTime for alternate package options.

Electrical Characteristics

All Min and Max limits are specified over temperature and rated operating voltage with 15 pF output load unless otherwise stated. Typical values are at 25°C and 3.3 V Vdd.

Table 1. Output Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Coverage						
Nominal Output Frequency Range	F_nom	1	–	60	MHz	Contact SiTime for higher frequency options
Temperature Range						
Operating Temperature Range	T_oper	-40	–	+85	°C	Industrial, ambient temperature
		-40	–	+105	°C	Extended industrial, ambient temperature
Rugged Characteristics						
Acceleration (g) Sensitivity, Gamma Vector	F_g	–	–	0.1	ppb/g	Low sensitivity grade; total gamma over 3 axes; 15 Hz to 2 kHz; MIL-PRF-55310, computed per section 4.8.18.3.1
Frequency Stability						
Frequency Stability over Temperature	F_stab	–	–	±10	ppb	Over -40 to 85°C operating temperature range (T_oper); referenced to (max frequency + min frequency)/2 over the temperature range. Contact SiTime for wider temperature ranges
		–	–	±20	ppb	Over either operating temperature range (T_oper); referenced to (max frequency + min frequency)/2 over the temperature range.
Initial Tolerance	F_init	–	±0.1	–	ppm	Initial frequency at 25°C at 48 hours after 2 reflows
Supply Voltage Sensitivity	F_Vdd	–	±1	–	ppb	Over operating temperature range (T_oper); Vdd ±5%
Output Load Sensitivity	F_load	–	±0.4	–	ppb	Over operating temperature (T_oper); LVCMOS output, 15 pF ±10%. Clipped sinewave, 10 kΩ || 10 pF ±10%
Frequency vs. Temperature Slope	ΔF/ΔT	–	±0.5	–	ppb/°C	0.5°C/min temperature ramp rate, -40 to 105°C
Dynamic Frequency Change during Temperature Ramp	F_dynamic	–	±0.004		ppb/s	0.5°C/min temperature ramp rate, -40 to 105°C
Hysteresis Over Temperature Contact SiTime for lower hysteresis	F_hys	–	±1		ppb	±10 ppb stability over temperature, 0.5°C/min ramp rate, defined as ±ΔF/2
		–	±2	–	ppb	±20 ppb stability over temperature, 0.5°C/min ramp rate, defined as ±ΔF/2
One-Day Aging	F_1d	–	±0.5	–	ppb	At 85°C, after 30-days of continued operation. Aging is measured with respect to day 31
One-Year Aging	F_1y	–	±100	–	ppb	At 85°C, after 2-days of continued operation. Aging is measured with respect to day 3
20-Year Aging	F_20y	–	±300	–	ppb	
20-Year Total Stability	F_tot_20y	-4.6		4.6	ppm	Complies with Stratum 3E per GR-1244-CORE. Actual performance is better
Allan deviation	ADEV	–	2e-11	–	–	10 second averaging time[4]
LVCMOS Output Characteristics						
Duty Cycle	DC	45	–	55	%	
Rise/Fall Time	Tr, Tf	0.8	1.2	1.9	ns	10% - 90% Vdd
Output Voltage High	VOH	90%	–	–	Vdd	IOH = +3 mA
Output Voltage Low	VOL	–	–	10%	Vdd	IOL = -3 mA
Output Impedance	Z_out_c	–	17	–	Ohms	Impedance looking into output buffer, Vdd = 3.3 V
		–	17	–	Ohms	Impedance looking into output buffer, Vdd = 3.0 V
		–	18	–	Ohms	Impedance looking into output buffer, Vdd = 2.8 V
		–	19	–	Ohms	Impedance looking into output buffer, Vdd = 2.5 V
Clipped Sinewave Output Characteristics						
Output Voltage Swing	V_out	0.8	–	1.2	V	Clipped sinewave output, 10 kΩ || 10 pF ±10%
Rise/Fall Time	Tr, Tf	–	3.5	4.6	ns	20% - 80% Vdd, F_nom = 19.2 MHz
Start-up Characteristics						
Start-up Time	T_start	–	2.5	3.5	ms	Time to first pulse, measured from the time Vdd reaches 90% of its final value. Vdd ramp time is 100 µs, 0 V to Vdd
Output Enable Time	T_oe	–	–	680	ns	F_nom = 10 MHz. See Timing Diagrams section below
Time to Rated Frequency Stability	T_stability	–	–	1.6	s	Time to first accurate pulse within rated stability, measured from the time Vdd reaches 90% of its final value. Vdd ramp time = 100 µs

Note:

4. Measured 2 hours after startup in a temperature chamber with a constant temperature in still air.

Table 2. DC Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply Voltage						
Supply Voltage	Vdd	2.25	2.5	2.75	V	Contact SiTime for 2.25 V to 3.63 V continuous supply voltage support
		2.52	2.8	3.08	V	
		2.7	3.0	3.3	V	
		2.97	3.3	3.63	V	
Current Consumption						
Current Consumption	Idd	–	44	53	mA	F_nom = 19.2 MHz, No Load
OE Disable Current	I_od	–	43	51	mA	OE = GND, output weakly pulled down

Table 3. Input Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Input Characteristics – OE Pin						
Input Impedance	Z_in	75	–	–	kΩ	Internal pull up to Vdd
Input High Voltage	VIH	70%	–	–	Vdd	
Input Low Voltage	VIL	–	–	30%	Vdd	
Frequency Tuning Range – I²C mode						
Pull Range	PR	±6.25 ±10 ±12.5 ±25 ±50 ±80 ±100 ±125 ±150 ±200 ±400 ±600 ±800 ±1200 ±1600 ±3200	–	–	ppm	Digitally controlled mode
Absolute Pull Range[5]	APR	±5.31	–	–	ppm	Over rated temperature range (T_rated); Digitally controlled mode for PR = ±6.25 ppm
		±5.26	–	–	ppm	Over operating temperature range (T_oper); Digitally controlled mode for PR = ±6.25 ppm
I²C Interface Characteristics, 200 Ohm, 550 pF (Max I²C Bus Load)						
Bus Speed	F_I2C	≤ 400			kHz	-40 to 105°C
		≤ 1000			kHz	-40 to 85°C
Input Voltage Low	VIL_I2C	–	–	30%	Vdd	Digitally controlled mode
Input Voltage High	VIH_I2C	70%	–	–	Vdd	Digitally controlled mode
Output Voltage Low	VOL_I2C	–	–	0.4	V	Digitally controlled mode
Input Leakage current	I_L	0.5	–	24	µA	0.1 V_{DD}< VOUT < 0.9 V_{DD}. Includes typical leakage current from 200 kΩ pull resister to VDD. Digitally controlled mode
Input Capacitance	C_{IN}	–	–	5	pF	Digitally controlled mode

Note:

5. APR = PR – initial tolerance – 20-year aging – frequency stability over temperature.

Table 4. Phase Noise

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Phase Noise						
1 Hz offset		–	-73	–	dBc/Hz	F_nom = 10 MHz Fixed frequency and digitally controlled mode with ±6.25 ppm pull range
10 Hz offset		–	-101	–	dBc/Hz	
100 Hz offset		–	-122	–	dBc/Hz	
1 kHz offset		–	-141	–	dBc/Hz	
10 kHz offset		–	-149	–	dBc/Hz	
100 kHz offset		–	-150	–	dBc/Hz	
1 MHz offset		–	-161	–	dBc/Hz	

Device Configurations and Pin-outs

Table 5. Device Configurations

Configuration	I²C Programmable Parameters
Fixed Frequency	–
Digitally Controlled	Frequency Pull Range, Frequency Pull Value, Output Enable control

Pin-out Top Views

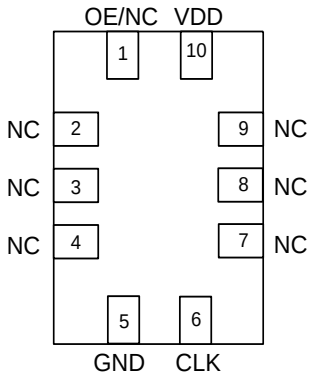


Figure 3. Fixed Frequency Device

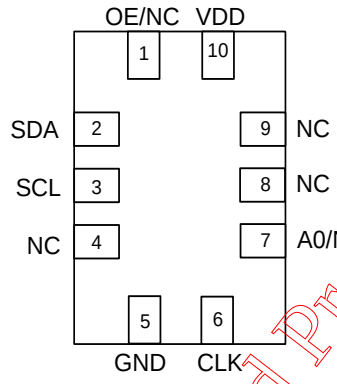


Figure 4. Digitally Controlled Device

Table 6. Pin Description

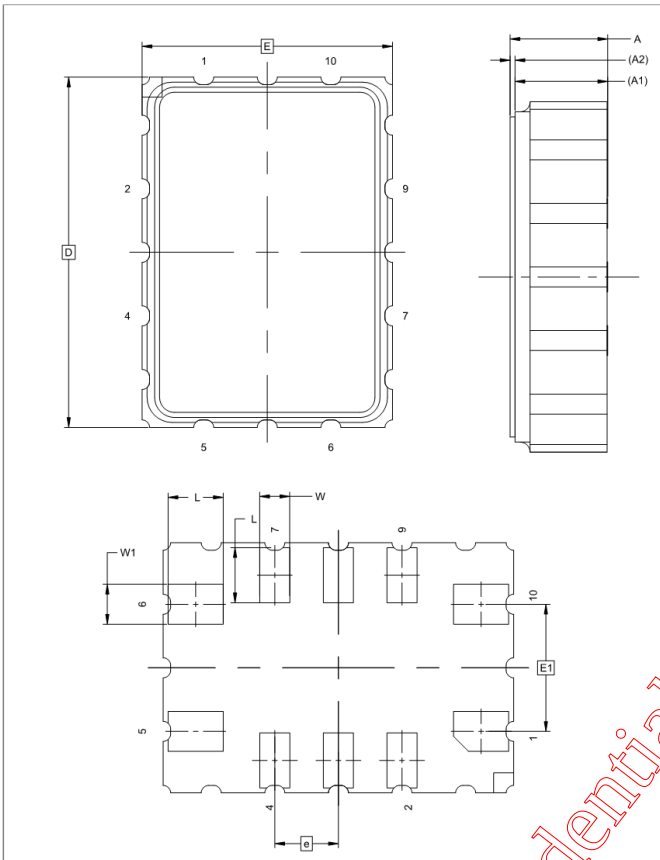
Pin	Symbol	I/O	Internal Pull-up/Pull Down Resistor	Function
1	OE / NC[8]	OE – Input	100 kΩ Pull-Up	H[6]: specified frequency output L: output is high impedance. Only output driver is disabled
		NC[7] – No Connect	–	H or L or Open: No effect on output frequency or other device functions
2	SDA / NC[8]	SDA – Input/Output	200 kΩ Pull Up	I²C Serial Data
		NC – No Connect	–	H or L or Open: No effect on output frequency or other device functions
3	SCL / NC[8]	SCL – Input	200 kΩ Pull-Up	I²C serial clock input
		No Connect		H or L or Open: No effect on output frequency or other device functions
4	NC[8]	No Connect	–	H or L or Open: No effect on output frequency or other device functions
5	GND	Power	–	Connect to ground
6	CLK	Output	–	LVCMOS, or clipped sinewave oscillator output
7	A0/NC[8]	A0 – Input	100 kΩ Pull-Up	Device I²C address when the address selection mode is via the A0 pin. This pin is NC when the I²C device address is specified in the ordering code. A0 Logic Level / I²C Address 0 / 1100010 1 / 1101010
8	NC[8]	No Connect	–	H or L or Open: No effect on output frequency or other device functions
9	NC[8]	No Connect	–	H or L or Open: No effect on output frequency or other device functions
10	VDD	Power	–	Connect to power supply[7]

Notes:

6. In OE mode for noisy environments, a pull-up resistor of 10 kΩ or less is recommended if pin 1 is not externally driven. If pin 1 needs to be left floating, use the NC option.
7. A 0.1 µF capacitor in parallel with a 10 µF capacitor are required between VDD and GND. The 0.1 µF capacitor is recommended to place close to the device, and place the 10 µF capacitor less than 2 inches away.
8. All NC pins can be left floating and do not need to be soldered down.

Dimensions and Patterns

Package Size – Dimensions (Unit: mm)



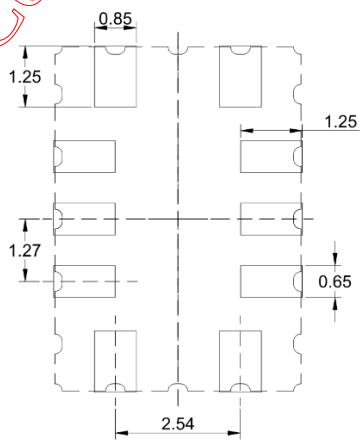
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A			2.2000
CERAMIC THICKNESS		A1		1.85 ref	
LID THICKNESS		A2		0.100 ref	
BODY SIZE	X	D		7 BSC	
	Y	E		5 BSC	
LEAD WIDTH		W	0.550	0.600	0.650
		W1	0.750	0.800	0.850
LEAD LENGTH		L	1.050	1.100	1.150
LEAD PITCH		e		1.27 BSC	
		e1		2.54 BSC	
PACKAGE EDGE TOLERANCE		aaa		0.150	
COPLANARITY		ccc		0.080	

NOTE

1. ALL DIMENSION IN MM

SiTime		
PKG INFO		DRAWING NO.
10L CQFN 7.000x5.00X2.2 mm		POD-086-CQFN-010-X7050
		REV / SHEET
DATE	6/30/2021	A00 / 01

Recommended Land Pattern (Unit: mm)



Note : All units in mm.

SiTime	PKG INFO	SPL DRAWING NO.	
	10L CQFN 5.000x7.000 mm	SPL-086-CQFN-010-C07050	
DATE		REV	SHEET
2021/06/16		Draft	01

Revision History

Table 7. Revision History

Version	Release Date	Change Summary
0.50	Apr 16, 2021	First release, preliminary information
0.51	Jul 14, 2021	Updated package ordering code, dimensions and patterns

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